University of Alberta

MAGNETICALLY ACTUATED CMOS MICROMACHINED CANTILEVER-IN-CANTILEVER DEVICES

by

YUAN MA

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of Master of Science

Department of Electrical and Computer Engineering

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ABSTRACT

Magnetically actuated micromachined Cantilever-In-Cantilever (CIC) devices are characterized and tested. Static deflection of the devices is estimated and verified by experimental results. Resonant response of the CIC structure is discussed and analysed. Thermal effects on the CIC structure are also considered and a temperature cooling phenomenon is explained.

A piezoresistive detection method is included and failures of the experiments are discussed.

A commercial finite element software package is used to simulate and analyse the static and resonant characteristics of the CIC devices.

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Contents

1 Introduction 1

1.1 Micromachining 1

1.2 CMOS Micromachining 2

1.3 Thesis Overview 2

2 CMOS Micromachining-Related Technologies 4

2.1 MOS Transistor Theory 4

2.2 CMOS Technology 7

2.3 A Typical CMOS Micromachining Fabrication Process 12

2.4 Wet Anisotropic Etching 14

2.4.1 CMOS micromachining anisotropic etching 15

2.4.2 Anisotropic etchants 17

3 Magnetically Actuated Micromachined Cantilever-In-Cantilever Devices 19

3.1 Design and Fabrication 19

3.1.1 The cantilever-in-cantilever structure 20

3.1.2 CIC design process 23

3.1.3 Fabrication of the triple CIC structure 24

3.1.4 Post-processing of the triple CIC structure 26

3.2 Static Deflection Calculation 27

3.2.1 Deflection of a single cantilever beam under a concentrated force 27

3.2.2 Deflection of a single cantilever beam under concentrated moment 31

3.2.3 Deflection of a triple cantilever-in-cantilever structure 32

3.2.4 Limitation of deflection calculation 36

3.3 Experiments and Analyses 37

3.3.1 Experimental set-up and optical detection method 38

3.3.2 Parameters for the deflection calculation 40

3.3.2.1 Layer thicknesses 40

3.3.2.2 Calculation of centroidal moment of inertia 41

3.3.2.3 External magnetic field 43

3.3.3 Comparison of the theoretical calculation with experiment results 44

3.4 Resonant Response 49
3.4.1 Uncoupled flexural equations of damped motion 49
3.4.2 Experiment results 49
3.4.3 Resonant frequency versus input currents 53
3.4.4 Lifetime testing of the CIC devices 54
3.5 Thermal Effects on the CIC Structure 55
3.5.1 Thermal actuation 55
3.5.2 Temperature effect at resonance 59
3.5.2.1 High vacuum testing system 60
3.5.2.2 Experimental results 61
3.6 Applications of the CIC Device 63

4 ANSYS Simulation **64**
4.1 Linear Static Analysis 66
4.2 Resonant Vibration Analysis 69

5 Piezoresistive Detection **72**
5.1 Piezoresistive Detection in CMOS Micromachining 73
5.2 Experimental Results 75

6 Conclusion and Outlook **78**

REFERENCES **80**

Appendices
Appendix A: Splus program example for static deflection calculation (n=4) 84
Appendix B: Input file for CIC ANSYS simulation 85

List of Tables

3.1 Mechanical properties of CMOS thin film materials 40

4.1 Natural frequencies of the triple CIC structures 69

List of Figures

2.1 Physical structure of an NMOS transistor 5

2.2 Physical structure of a PMOS transistor 6

2.3 Physical structure of a CMOS inverter 7

2.4 A typical n-well CMOS process 10

2.5 Cross-section of a wafer of a typical CMOS micromachining fabrication 13

2.6 A summary of wet anisotropic etching on a (100) surface 15

2.7 Wet anisotropic etching procedure for releasing a cantilever beam 16

3.1 SEM picture of a quadruple CIC device 20

3.2 Triple Cantilever-In-Cantilever plan view and metal layers arrangement 22

3.3 Triple Cantilever-In-Cantilever layout 25

3.4 Single prismatic beam under concentrated force P 27

3.5 Free-body diagram of partial cantilever beam 28

3.6 Single prismatic beam under concentrated moment M 31

3.7 Free-body diagram of three cantilevers of a CIC structure 33

3.8 SEM picture of a group of cantilevers 37

3.9 Experimental set-up for the deflection measurement 38

3.10 Deflection angle illustration 39

3.11 Layer thickness of Mitel 1.5 μm micromachined structure 41

3.12 Cross-section of a typical supporting arm of a cantilever structure 42

3.13 Conceptual diagram of the region with uniform magnetic field 44

3.14 Deflection of a series of CIC structures 45

3.15 SEM picture of a sliced Mitel chip 47

3.16 Total deflection variation with AC and DC current 48

3.17 Resonant response of a triple CIC structure without field oxide layer 50

3.18 Frequency response experiment to determine damping ratio 51

3.19 Deflection curve near resonance 52

3.20 Resonant frequency changing versus input current 53

3.21 Resonant frequency variation versus temperature increase 54

3.22 Thermal effect of a triple CIC actuation 56

3.23 Deflection of a triple CIC structure without thermal effects 57

3.24 Total deflection of a triple CIC structure 58

3.25 Temperature increase of the support arms versus driving frequency 60

3.26 Conceptual diagram of the vacuum system 61

3.27 Temperature variation under atmospheric pressure and 2×10^{-5} Torr 62

4.1 Three dimensional mode built for cantilever structure 65

4.2 Deformed shape of a CIC structure 66

4.3 Deflection shape of a CIC structure 67

4.4 Comparison of ANSYS simulation with experiment 68

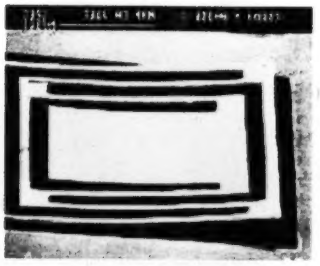
4.5 Vibration modes of triple CIC structure (A) f=6.70 kHz: (B) f=8.27 kHz; (C) f=18.87 kHz; (D) f=29.89 kHZ 70

5.1 Conceptual diagram of a CIC structure with piezoresistor embedded inside the supporting arms 73

5.2 Piezoresistance versus current in aluminum lead 75

5.3 Resistance variation of piezoresistor without thermal effects 76

1



Introduction

1.1 Micromachining

The term *micromachining* originally came from Japan[1]. It is referred to as microsystems in Europe and Microelectromechanical system (MEMS) in North America.

Micromachining represents a new class of systems which differ from classical technical systems by the fact that they use microfabrication technologies for their manufacturing. In other words, the process of manufacturing is in the micrometer range of dimensions. Compared to its macro-size counterparts, micromachining has the advantages in size, weight, geometrical accuracy, reproducibility, reliability and cost.

In terms of its final products, micromachining can be classified as bulk micromachining or surface micromachining[2]. Bulk micromachining depends on the mechanical properties of single-crystal silicon and is usually performed by selectively etching crystalline silicon[3]. The structures developed with bulk micromachining are made

of either crystalline silicon or deposited or grown films on silicon. Surface micromachining refers to the fabrication of three-dimensional micromechanical structures from multiple stacked and patterned thin films[4].

1.2 CMOS Micromachining

About one decade ago, Parameswaran, *et al.* combined a standard CMOSIC (Complementary Metal Oxide Silicon Integrated Circuit) process with micromachining and formed a new branch of micromachining: CMOS micromachining[5-8]. Standard CMOS processes are used to build a structure with exposed silicon substrate and electrical circuits. The micromachining process etches underneath the structure from the exposed substrate area to release the structure. Compared to the other non-standard microfabrication methods, CMOS micromachining has the advantages of high degree of reliability and repeatability because of well-defined process parameters. CMOS micromachining also makes it possible to merge integrated circuits and micromechanical structures on the same chip.

Furthermore, standard commercialized CMOS processes can be accessed by universities through the Canadian Microelectronics Corporation (CMC) in Canada. This access provides a fruitful environment for CMOS micromachining research and development.

1.3 Thesis Overview

CMOS micromachining technology research and applications have grown rapidly in recent years and have become a simple but powerful approach especially applicable for bulk micromachining. A major driving force in this development has been the application of

micromachining to sensors and actuators, something now in great demand by industry. Until recently CMOS micromachining has been primarily restricted to the production of static devices or devices displaying little spatial displacement. The main problem of fabricating dynamic structures using standard processes is the difficulty of finding a suitable way to actuate the mechanical structures. Most reported movable structures realized using CMOS technologies are thermally activated[9-14] since thermally sensitive materials can be easily found in standard CMOS fabrication processes. The disadvantages of thermal actuation, however, are slow response time, unidirectional motion and small deflection angles.

Novel, magnetically actuated CMOS-compatible micromachined devices have been invented in our Micromachining Application and Development Laboratory of the University of Alberta[15-17]. Actuation is produced by Lorentz forces arising from the interaction between the currents flowing in the structure and an external magnetic field.

In this thesis, the research is aimed at characterization of the deflection and verification of resonant vibration features of the magnetically actuated devices mentioned above.

In Chapter 2, several CMOS micromachining-related processes are introduced after a general introduction of MOS transistor theory.

The design and fabrication of a particular device, based on a cantilever-in-cantilever construction, will be introduced in Chapter 3. An estimation of the static deflection, together with the resonant response will also be included. The last section of Chapter 3 concentrates on the thermal and temperature effects of the device and a vacuum testing system is used to test our results.

Chapter 4 reports the simulation results of the devices. ANSYS, a commercial finite element package available from Swanson Software is used to simulate the static deflection and resonant vibration of the device.

In Chapter 5 a piezoresistance detection method is described and Chapter 6 discusses some conclusions reached. Finally, an outlook for future research is given.

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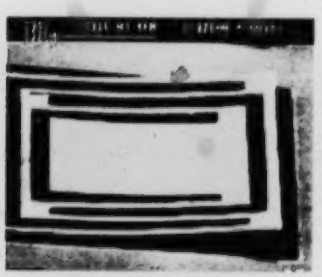


CMOS Micromachining-Related Technologies

CMOS technology is the base of CMOS micromachining. In this chapter several microelectronic processes in CMOS technology are introduced after a general introduction of MOS transistor theory. A typical CMOS micromachining process including CMOS fabrication and wet anisotropic etching is also introduced.

2.1 MOS Transistor Theory

Part of this section comes from a course report[18] of the author.

A MOS transistor is termed a majority-carrier device in which the current in a conducting channel between the source and the drain is modulated by a voltage applied to the gate[19]. In an n-type MOS transistor (i.e., NMOS), the majority charge carriers are

electrons. A positive voltage applied to the gate with respect to the substrate enhances the number of electrons in the channel (the region immediately under the gate) and hence increases the conductivity of the channel. For gate voltages less than a threshold value, denoted by V_t, the channel is cut off causing a very low drain-to-source current. The operation of a p-type transistor (i.e., PMOS) is analogous to the NMOS transistor, with the exception that the majority carriers are holes and the voltages are negative with respect to the substrate.

Figure 2.1 and Figure 2.2 show the physical structures of an NMOS transistor and a PMOS transistor. In the moderately doped p-type substrate in Figure 2.1 there are two heavily doped n^+ regions, the source and the drain. Between these two regions there is a narrow p-type region called the channel which is covered by a thin insulating layer of silicon dioxide, called the gate oxide. Over this oxide layer is a polycrystalline silicon (polysilicon) electrode referred to as the gate. The oxide layer is an insulator and therefore the DC current from the gate to the channel is essentially zero. Because of the inherent symmetry of the structure there is no physical distinction between the drain and source regions.

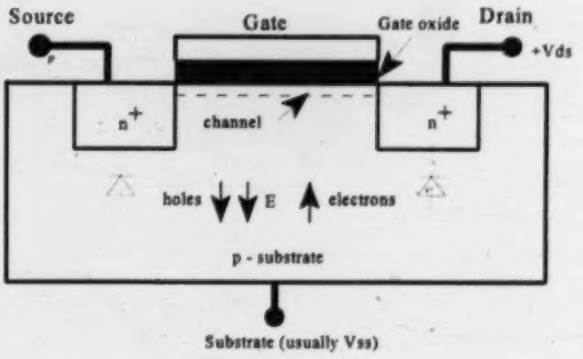


Figure 2.1 Physical structure of an NMOS transistor

In operation a positive voltage is applied between the source and the drain. With zero gate bias no current flows from source to drain because they are effectively insulated from each other by the two reverse-biased pn junctions. However, when a voltage positive with respect to the source and the substrate is applied to the gate, it produces an electric field E across the substrate which attracts electrons towards the gate and repels holes. If the gate voltage is sufficiently large, the region under the gate changes from p-type to n-type and provides a conduction path between the source and the drain. Under these conditions the surface of the underlying p-type silicon is said to be inverted.

Similar to the NMOS transistor, a conduction path is created between the source and the drain of a PMOS transistor in Figure 2.2 when a voltage negative with respect to the source and the substrate is applied to the gate. However, in this instance conduction results from the movement of holes in the channel. A negative drain voltage sweeps holes from the source through the channel to the drain.

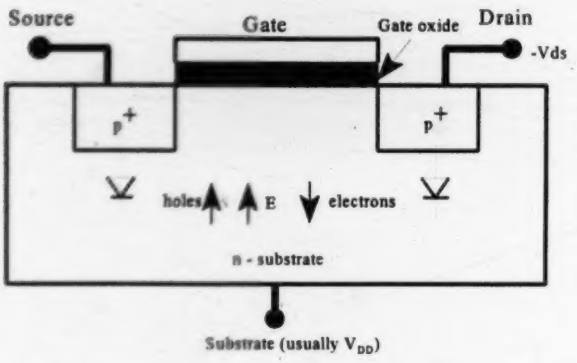


Figure 2.2 Physical structure of a PMOS transistor

2.2 CMOS Technology

Over the past decade Complementary Metal Oxide Silicon (CMOS) technology has played an increasingly important role in the global integrated circuit industry. In CMOS technology, both NMOS and PMOS transistors are fabricated on the same silicon substrate to achieve low power dissipation. Figure 2.3 shows the physical structure of a CMOS inverter.

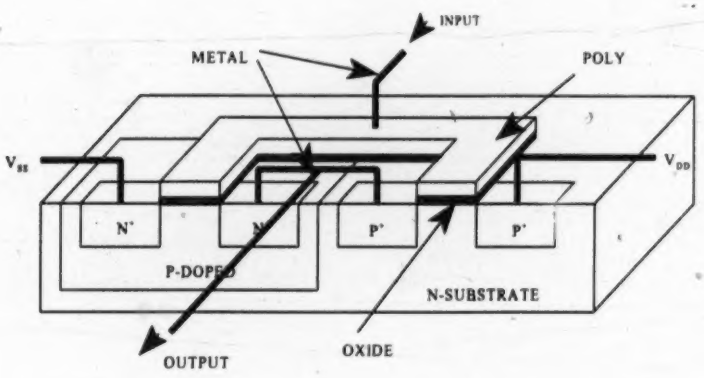


Figure 2.3 Physical structure of a CMOS inverter

CMOS technology is most widely used today. In CMOS technology, there are four main processes[19]:

- n-well process
- p-well process
- twin-tub process
- silicon-on-insulator process

In the n-well process, for example, a common approach has been to start with a lightly doped p-type substrate, create the n-type well for the p-channel devices, and build the n-channel transistor in the native p-substrate. Figure 2.4 illustrates the major steps involved in a typical n-well CMOS process with only one metal layer.

• The first mask defines the n-well, in which p-channel transistors will be fabricated. Ion implantation or deposition and diffusion are used to produce the n-well (Fig. 2.4 a).

•The next mask is called the "active area" mask. It defines where areas of thin oxide are needed to implement transistor gates and allow implantation to form p- or n-type diffusions for transistor source/drain regions (Fig. 2.4 b). A thin layer of SiO_2 is grown and covered with Si_3N_4 which is used as a masking layer for the following two steps.

• The next step is the channel-stop implantation. It uses a photoresist mask and dopes the p-substrate by boron implantation in areas where there are no n-transistors (Fig. 2.4 c). This, in conjunction with the thick field oxide that will cover these areas, aids in preventing conduction between unrelated transistor source/drains.

• The photoresist mask is then stripped leaving the previously masked SiO_2/Si_3N_4 sandwich defining the active regions. A thick field oxide is then grown in both the vertical and lateral directions (Fig. 2.4 d). This general oxide construction technique is called Local Oxidation of Silicon (LOCOS).

• An n/p-transistor threshold voltage adjust step might then be performed by doping using a p/n-well photoresist mask[19].

• Polysilicon gate definition is then completed (Fig. 2.4 e).

• An n^+ mask is then used to define those thin-oxide areas that are to be n^+ implanted (Fig. 2.4 f). In the modern small-dimension process the Lightly Doped Drain structure (LDD) is used to reduce hot carrier effects (Fig. 2.4 g). This consists of a shallow n-LDD implant that covers the source/drain region where there is no polysilicon. A spacer oxide is then grown over the polysilicon gate and followed by an n^+ implant to produce n^+ regions that are spaced from the edge of the original poly gate edges. The spacer is then removed resulting in a structure that is more resistant to hot-electron effects.

• In the next step the complement of the n^+ mask is usually used. It defines the area

of a p^+ diffusion or p-active region (Fig. 2.4 h). Following this step the surface of the wafer is covered with a layer of SiO_2.

• Contact cuts are then defined (Fig. 2.4 i). This involves etching any SiO_2 down to the surface to be contacted. It allows metal to contact diffusion or polysilicon regions.

•The wafer is metallized and selectively etched to produce circuit interconnections (Fig. 2.4 j).

• As a final step the wafer is protected by a passivation layer consisting of sandwiched SiO_2 and Si_3N_4 layers and openings to the bonding pads are etched to allow for wire bonding. The passivation layer protects the silicon surface against the ingress of contaminants such as sodium and water vapor (not shown in Fig. 2.4).

Through the CMC (Canadian Microelectronics Corporation) the university communities have access to the following CMOS processes:

- Mitel 1.5 micron CMOS Process
- Northern Telecom CMOS4S 1.2 micron Process
- Northern Telecom 0.8 micron BiCMOS Process

Detailed process descriptions and step-by-step illustrations can be found in references [20-22].

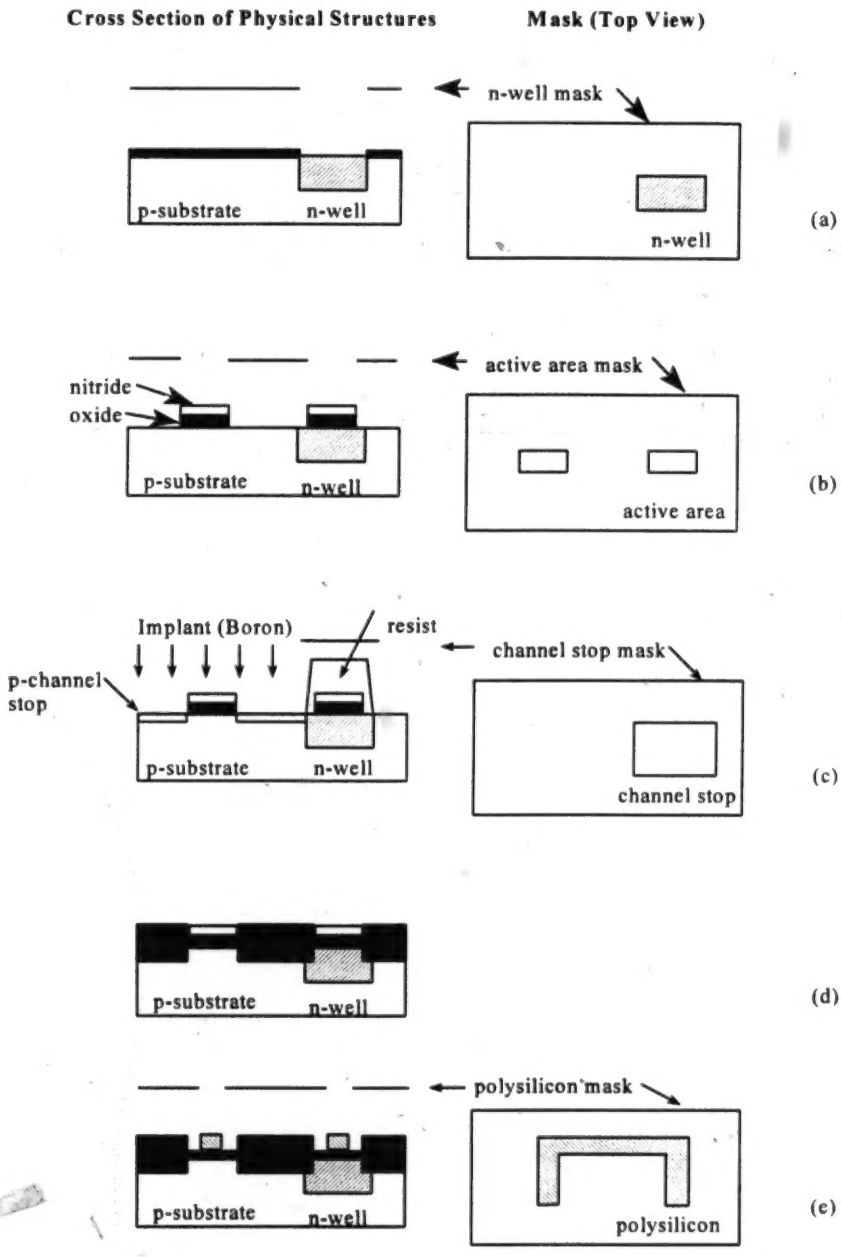


Figure 2.4 A typical n-well CMOS process

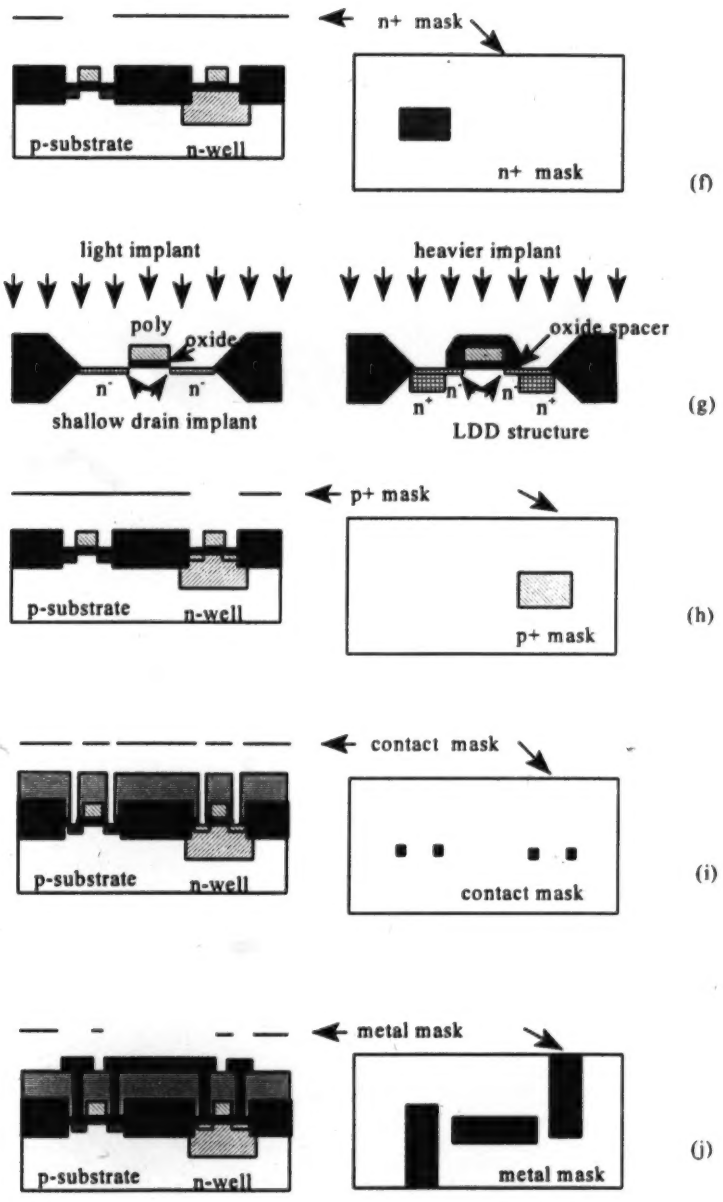


Figure 2.4 A typical n-well process (continued)

2.3 A Typical CMOS Micromachining Fabrication Process

CMOS micromachining is a combination of the standard CMOS process and silicon micromachining technology.

First, the standard CMOS process is used to build the structure with electric circuitry and create an opening on the substrate by making all the films absent at that region. This implies that the layers of the active area, contact cut, via, and passivation should be stacked in the layout design, resulting in no layers being deposited at these locations on the fabricated wafers. A bulk micromachining process is then used to remove the exposed silicon substrate and release the structure.

Bulk silicon micromachining may use wet anisotropic etching to fabricate well-defined three-dimensional micromechanical structures in silicon, polysilicon and silicon oxides and nitride. Details about anisotropic etching are given in section 2.4. In this section a typical CMOS micromachining fabrication process making use of the Mitel 1.5 micron process is given to illustrate the general procedure of fabricating CMOS micromachined devices. It should be noted that both Mitel 1.5 micron and Nortel CMOS4S 1.2 micron processes were used to fabricate the devices discussed in this thesis. The main differences of the above two processes are layer thickness and material parameters.

A typical CMOS micromachining fabrication process may include the following steps. Figure 2.5 shows a cross-section of the layers. Vertical dimensions are obtained from the Mitel 1.5 micron process data[20].

• Highly conductive n+ doped layers are diffused over the n-wafer. The Mitel 1.5 micron process is a p-well-based process starting with an n-type wafer. On the other hand, the Nortel CMOS4S process is an n-well-based process starting with a p-type wafer. Both processes have two polysilicon layers and two metal layers.

• A 0.9 μm field oxidation layer may be used as a dielectric layer which electrically isolates the polysilicon structure from the crystalline substrate after initial oxidation and P-well diffusion. It may also be used as structural material. This field oxidation layer may be etched a little during the following steps, which means a thickness smaller than 0.9 μm is possible.

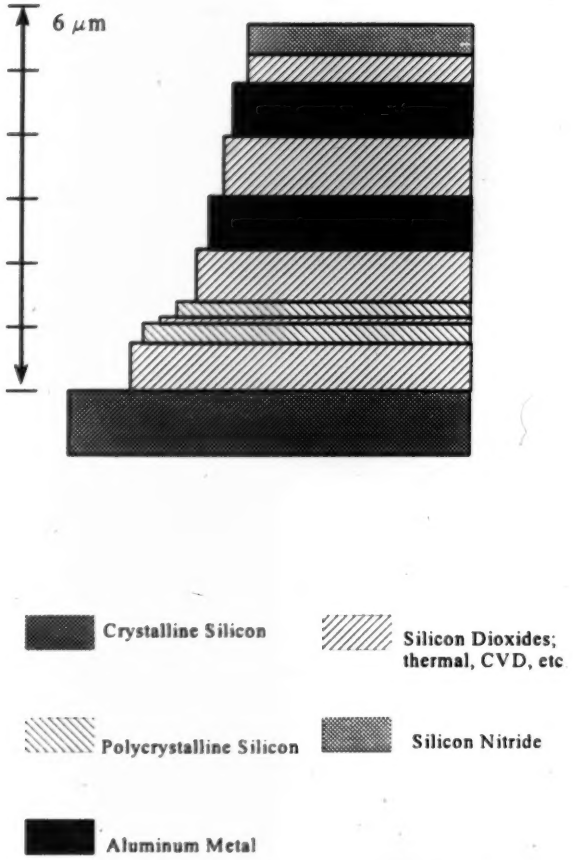


Figure 2.5 Cross-section of a wafer of a typical CMOS micromachining fabrication

• After pre-gate oxidation and gate oxidation (about 0.027 μm, not shown in Figure 2.5), two layers of low-stress doped polysilicon are then deposited (about 0.32 μm and 0.25 μm respectively) with a 0.02 μm oxide layer between. There may be two or three of these polysilicon layers depending on the technology. Furthermore, polysilicon layers can also be used as electrically conductive layers.

• Then a 0.8 μm dielectric layer mainly composed of low-stress sacrificial phosphosilicate glass (PSG) is deposited.

• Two 0.8 μm-thick patterned aluminum layers are used to form conducting layers and for electrical interconnects. There is a 1.0 μm inter-dielectric layer between two metal layers.

• Finally, a layer of passivation (0.5 μm oxide and 0.5 μm nitride) is deposited.

2.4 Wet Anisotropic Etching

Wet anisotropic etching is a process of preferential directional etching of material using liquid etchants. The precise mechanisms underlying the nature of wet anisotropic etching are not well understood but etch rates are dependent on the crystallographic orientation of the material. As well, the etching process is fundamentally a charge-transfer procedure and the etch rates are dependent on dopant type and concentration of the material to be etched. The principal feature of anisotropic etching in silicon is that (111) surfaces are attacked at a much slower rate than all other crystallographic planes. It may be due to (111) silicon surfaces exhibiting the highest density of atoms. Further explanation can be found in reference [23].

2.4.1 CMOS micromachining anisotropic etching

Anisotropic etching is a particularly useful tool in micromachining. Since (100) wafers are exclusively used in CMOS technologies, Figure 2.6 gives a summary of wet anisotropic etched holes on a (100) surface.

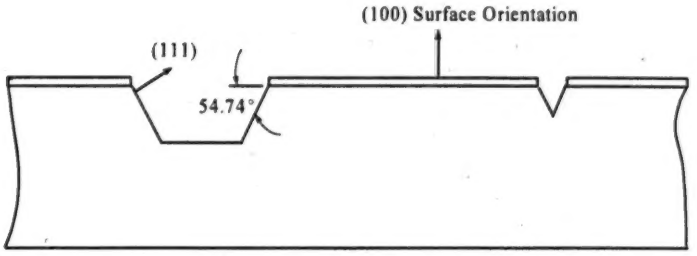


Figure 2.6 A summary of wet anisotropic etching on a (100) surface

First, the (100)-oriented silicon chip is patterned by a mask layer to make certain areas of the silicon substrate exposed. Then the chip is dipped into a wet anisotropic etchant for a period of time. The final etched pit is bounded by (111) crystallographic surfaces as shown in Figure 2.6.

For a more complicated mask geometry shown in Figure 2.7, undercutting of the mask plays an important role. Undercutting occurs when the (111) surfaces or vertical etch stop layer (such as a heavily doped boron-doped buried layer which will limit further downward etching) are encountered. Any mask opening containing a convex corner will also produce undercutting of the region beneath the mask.

Figure 2.7 shows the anisotropic etching process of a released single cantilever. In the beginning the silicon substrate is etched downward until (111) surfaces are encountered (see Figure 2.7 (a)). Simultaneously, the convex corners are undercut by anisotropic etchant

at a rate determined by the magnitude of the maximum etch rate and etch ratios for various crystallographic planes (see Figure 2.7(b)). If the silicon is etched long enough, convex corners will continue to be undercut until the pit eventually becomes pyramidal and bounded by the (111) surfaces (see Figure 2.7(c)). The cantilever beam has been released.

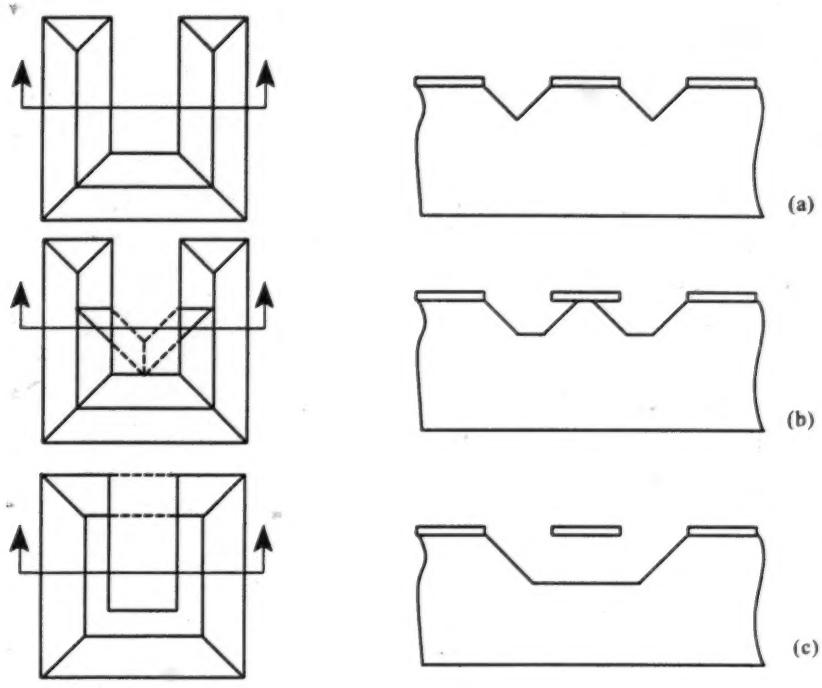


Figure 2.7 Wet anisotropic etching procedure for releasing a cantilever beam

Since the openings in the mask can only support a certain flux of etchant, the undercutting may be reduced by using a mask with very narrow openings when undercutting is not wanted. Sometimes, if the openings in the mask are not big enough or the etching time is not long enough, the silicon substrate beneath the cantilever beam may not be etched completely. One device discussed in this thesis also has this problem, resulting in a partially etched pillar of silicon beneath, but unattached to, the cantilevers. The unetched silicon underneath is difficult to detect since the cantilever contains one or more metal layers and is therefore opaque.

2.4.2 Anisotropic etchants

All the chips referred in this thesis are etched using an Ethylene Diamine Pyrocatechol (EDP) solution containing 750 mL ethylene diamine (NH_2-CH_2-CH_2-NH_2), 240 g pyrocatechol ($C_6H_4(OH)_2$), 240 mL DI water and 6 g pyrazine ($C_4H_4N_2$)[23].

Ethylene diamine pyrocatechol is a well-established anisotropic etchant for micromachining and is described in detail in the literature [24-28]. The main advantages of EDP are:

- EDP is an anisotropic etchant, which makes it possible to realize an etching with distinct geometries.
- EDP is highly selective and can be masked by a variety of materials, e.g., SiO_2, Cr and Au.
- The EDP etch rate is dopant dependent. The etch rates of silicon which has been highly doped with boron is near zero, so the heavily boron-doped buried layer may be used as vertical etch stop layer.

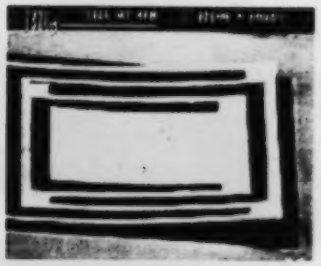
There are four types of commonly used EDP etchant solutions different in composition: type T, S, F and B[27]. The different types of EDP solutions have different etching rates and etching qualities, but all EDP types have an excellent selectivity with respect to the silicon dioxide and nitride layers. The etching ratio of silicon to oxide is about 10^4 :1. B-type etchant is used for all the chips discussed in this thesis. The etch rate for silicon is about 1.4-1.6 μm/min in the <100> direction at 119 °C. The etch rate for aluminum on unprotected bonding pads is about 180 times lower, and that of the silicon dioxide is about 10 nm/hr.

A silicon surface exposed to the air immediately grows a thin oxide layer. Thus the wafers have to be dipped in a buffered oxide etch (BOE) for 10-15 seconds to remove the native oxide built up on the silicon surface just before the anisotropic etching. Otherwise, a very rough surface will be produced and it is difficult to estimate the etching time if the native oxide is not removed first.

EDP is difficult to use because it is toxic and is even suspected to be carcinogenic. Moreover, EDP mixtures should be kept under a pure nitrogen atmosphere. Exposing them to oxygen forms benzoquinone, which leads to an uncontrollable increase of the etch rate and a darkening of the solution.

Recently, Tetra methyl ammonium hydroxide ($N(CH_3)_4OH$) and water (TMAHW) have been extensively studied by O. Tabata, *et al.*[29-30]. Passivation of aluminum may be achieved by adding a certain amount of silicon to the etch solution. The amount of silicon added depends on the TMAH concentration. Hopefully, TMAH can replace EDP to be used widely in CMOS micromachining etching processes. But unfortunately, anisotropic etching with TMAH has not been successfully realized by the author because of the inaccurate amount of silicon added to the solution. The bonding pads of the chip etched by TMAH could not be protected effectively.

3



Magnetically Actuated Micromachined Cantilever-In-Cantilever Devices

Micromachined silicon dioxide cantilever beams have been largely used as sensor structures since the development of controlled anisotropic etching[3]. Substantial literature exists in the area of pressure transducers, accelerometers, electromechanical switches etc. In this chapter, a novel cantilever-in-cantilever (CIC) device capable of large deflection angles is introduced, characterized and tested. Applications of the device conclude this chapter.

3.1 Design and Fabrication

The magnetically actuated cantilever-in-cantilever device is fabricated by combining "standard" CMOS technology, as introduced in Chapter 2, with silicon micromachining techniques. The etching properties of the (100) silicon substrate and the features of CMOS technology allow the fabrication of micromechanical structures based on the dielectric layers of silicon dioxide and silicon nitride by an anisotropic etching step performed after the

completion of the CMOS IC process.

3.1.1 The cantilever-in-cantilever structure

For Very Large Scale Integrated Circuit (VLSI) design and micromachining design, there are several CAD tools available: KIC, Electric, Vivid, Cadence and other commercial software. However, most of them are expensive and are designed for workstations running in a UNIX environment. Here, L-Edit, a product of Tanner Research Inc., which can be used conveniently under Microsoft Windows 3.x or IBM OS/2 2.0 is used for the design of the CIC structure.

Figure 3.1 is a scanning electron micrograph of a quadruple CIC device. The device is composed of four cantilevers. The central cantilever is embedded in the surrounding

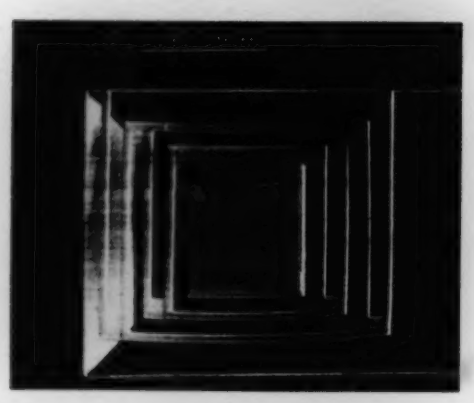


Figure 3.1 SEM picture of a quadruple CIC device

cantilever, which is in turn embedded in the other three surrounding cantilevers. The central cantilever is 240 μm × 260 μm. The central plate has an electrically isolated metal layer and is used as a mirror plate for reflecting a laser beam during optical measurements. The cantilever arms are about 15 μm wide and consists of a sandwich of field oxide, metal, CVD oxide and nitride.

The width of the anisotropically etched trough beneath the structure is about 400 μm wide and 50 μm deep after 75 minutes of etching in 119°C EDP. The length of the trough is about 2000 μm. Four devices fit in the same trough. Experimental results showed that the long trough has a better undercutting of silicon substrate than separate pits.

A SEM picture of a triple CIC device can be seen as the header of every chapter of this thesis. Compared with the quadruple CIC structure, the triple CIC has a larger ratio of reflection area to the whole device area. Most of the work reported here is concentrated on the triple CIC. Figure 3.2 is a plan view of the triple CIC structure. The actuation of the device is produced by Lorentz forces arising from the interaction between an external magnetic field ($\vec{B}$) and the current (I_e) flowing in the cantilever beams:

$$\vec{F} = I_e \vec{l} \times \vec{B} \qquad (3.1.1)$$

in which I_e is the electrical current, $\vec{B}$ is the external magnetic field, $\vec{l}$ is the length of a straight line segment of current in the cantilever and $\vec{F}$ denotes the Lorentz force on that segment.

From Figure 3.2 the principle of the CIC actuation can be seen: if an external magnetic field B is applied in the plane of the substrate and parallel to the cantilever arms, Lorentz forces will occur only on the segments at the ends of the cantilevers with opposite directions when there is a current flowing inside the structure. There are no Lorentz forces on the arms of the cantilevers. In Figure 3.2, ⊗ indicates the Lorentz force directed into the paper and ⊙ indicates the Lorentz force directed out of the paper.

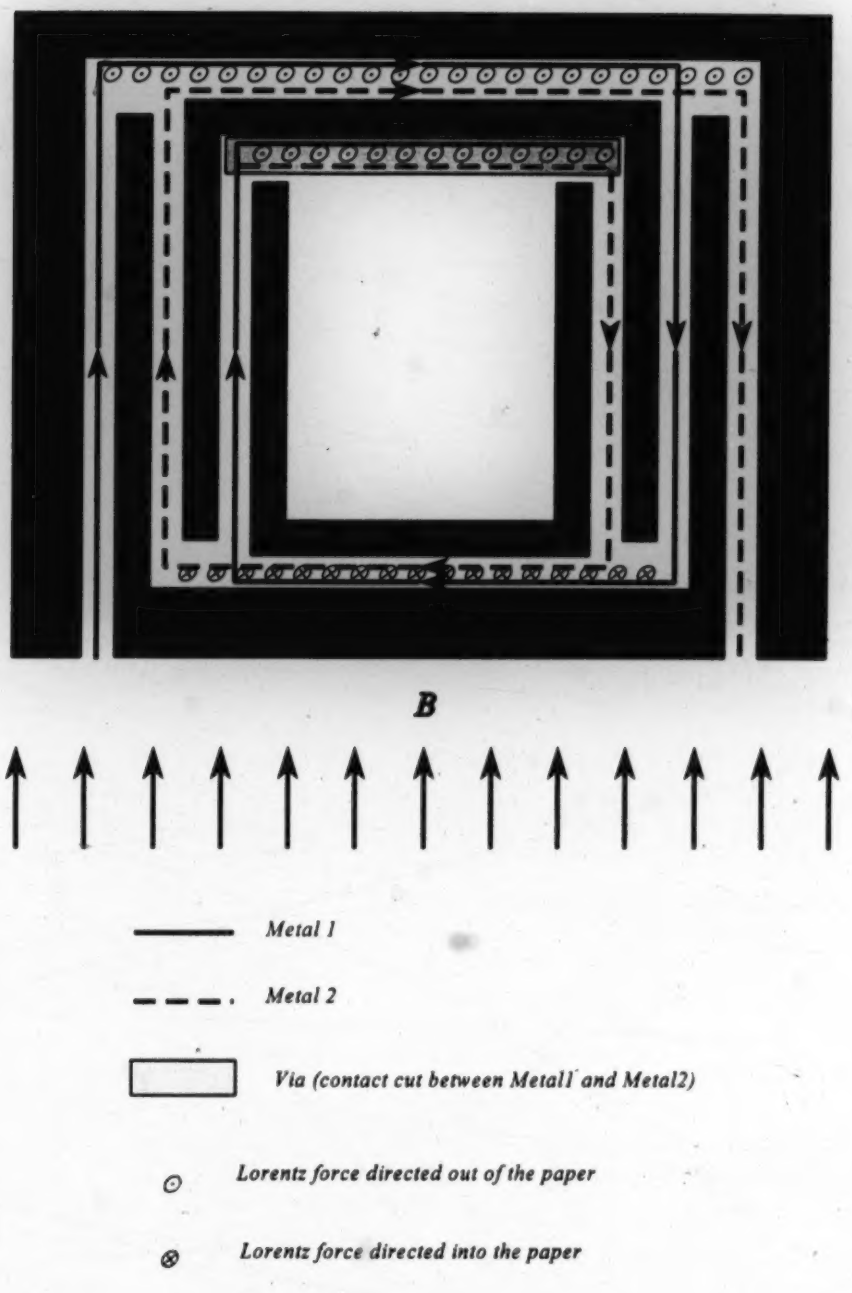

B
Metal 1
Metal 2
Via (contact cut between Metal1 and Metal2)
Lorentz force directed out of the paper
Lorentz force directed into the paper

Figure 3.2 Triple Cantilever-In-Cantilever plan view and metal layers arrangement

Two metal layers are used to increase the actuation of the CIC devices. In the region of Figure 3.2 where two metal leads are side-by-side, they actually overlap each other in the real device but are electrically isolated from each other. Two metal layers are joined together by the via at the end of the central cantilever. If an AC current is applied, the device will oscillate with the applied frequency. At their resonant frequencies, triple CIC devices may have deflections up to 65°. In the rest of this chapter and Chapter 4, more detailed research will be introduced on the deflection and resonance characteristics of CIC devices.

3.1.2 CIC design process

The design process of the CIC structure is introduced in this section. L-EDIT is used to lay out the structure layer by layer. Figure 3.3 is the final layout of a triple CIC structure.

1. In the first step, the **Active Area** is drawn to define the area where field oxide will not be grown. It provides the basic shape of the anisotropic etching opening. See Figure 3.3 (a). Before going to the next layer, an etch stop protection structure may be considered[31]. Usually a region of heavily p-doped silicon can be used as an etch stop barrier during an anisotropic etch. Therefore, a region without field oxide surrounding the structure just created should be introduced as shown also in Figure 3.3 (a). It will be used for the p^+ doping discussed in the next step. This etch stop protection structure is optional. Some devices designed without this etch stop protection didn't show problems during etching.

2. If you did not choose the etch stop protection in the first step, omit this step. Otherwise, the p+ doping region should be drawn out in the second step. Select the **P^+ Doping** layer and draw a frame covering the protection frame of the Active Area as shown in Figure 3.3 (b).

3. The next layer is the **Contact Cut**. In addition to being used to define the contact cut region, the Contact Cut layer is also used to expose the silicon substrate by overlapping

on the Active Area layer. Figure 3.3 (c) shows a Contact Cut layer overlapping the Active Area layer.

4. The layer of **Metal1** is used to form a part of the coil conducting current around the peripheries of the cantilevers as well as the mirror plate on the surface of the central cantilever. See Figure 3.3 (d).

5. Two metal layers are connected by the **Via** layer. The Via is at the end of the central cantilever and it is symmetric to the x-axis to keep the structure symmetric. The Via layer is also used to overlap the Active Area to permit exposure of the silicon substrate for etching. See Figure 3.3 (e).

6. The rest of coil uses the **Metal2** layer to complete the circuit around the periphery of the device. Two layers of metal increase the actuation forces. See Figure 3.3 (f).

7. The last layer is the **Passivation** layer. It overlaps the Active Area, Contact Cut layer and the Via layer to avoid the silicon dioxide and nitride deposition. See Figure 3.3 (g).

Detailed design steps can be found in reference [18].

3.1.3 Fabrication of the triple CIC structure

The device may be fabricated using the Northern Telecom CMOS4S technology or Mitel 1.5 micron CMOS technology through the Canadian Microelectronics Corporation (CMC).

The layout data are submitted to the industrial foundries in Caltech Intermediate Format (CIF) file.

As introduced in Sec. 3.1.2, by superposition of the active area layer, the contact cut layer, the via layer and the passivation layer, all oxide and passivation layers are removed during the CMOS fabrication, exposing portions of the silicon substrate as designed.

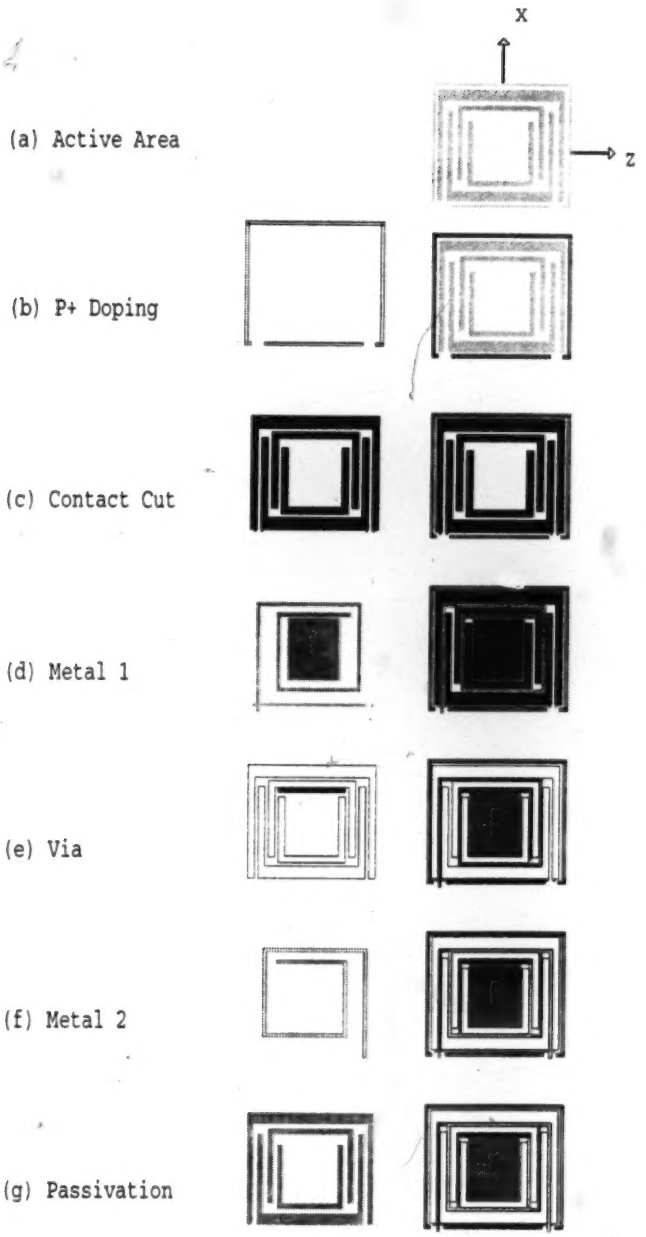


Figure 3.3 Triple Cantilever-In-Cantilever layout

3.1.4 Post-processing of the triple CIC structure

Anisotropic etching is one of the post-processing steps. Such steps may include the deposition of specific sensor materials, a cleaning process or a final cut of the wafers to obtain single devices. All these steps have to be compatible with the foregoing CMOS process and must not affect either the electrical circuitry or the function of the device.

The anisotropic etching of the devices is done at the Alberta Microelectronic Centre (AMC). The etchant used is an Ethylene Diamine Pyrocatechol (EDP) solution (for details, see Sec. 2.4.2). The chip received from CMC is etched for about 75 minutes at 119 °C. The etchant etches the silicon substrate exposed by the above design and fabrication process.

From the results of our experiment, the Mitel process is strongly resistant to EDP etching of the inside corners of the structure. During optical inspection, a distinct layer of residue is visible in the corners and along the edges of the active areas on some die batches. It appears clear or light grey and probably is an oxide of some sort. Due to this oxide residue in the exposed area, it takes more than 75 minutes in 119 °C EDP to release the structure completely, which may cause a problem with the exposed metal pads. Etching of aluminum from the side of the supporting arms by seepage between the oxide layers may also occur. All these lead to a lower yield of the post-processing. The dimensions of the CIC devices may also decrease because of a long etching time, which will affect the mechanical characteristics of the devices directly, although we have not investigated this aspect. The reason for the fabrication residue may be due to imperfect alignment of four mask layers (active area, contact cut, via and passivation layers). Although this method of exposing the silicon substrate is commonly used in CMOS micromachining, it violates the design rules of CMOS technologies badly. A few improvements of the design rule violations are discussed in the last Chapter.

Moreover, the CIC structure, including the mirror plate, has a cylindrical curvature due to inherent stress after etching. This may be seen in the SEM pictures.

3.2 Static Deflection Calculation

Deflection of a single cantilever beam of uniform cross section and carrying a load **P** at its free end is a common problem in Mechanics. The equation of the elastic curve and the angle of the deflection can be deduced by integration. In this section, static deflection of a triple cantilever-in-cantilever structure will be estimated from the results of a single cantilever beam.

3.2.1 Deflection of a single cantilever beam under a concentrated force

Figure 3.4 shows a single cantilever beam under a concentrated force P.

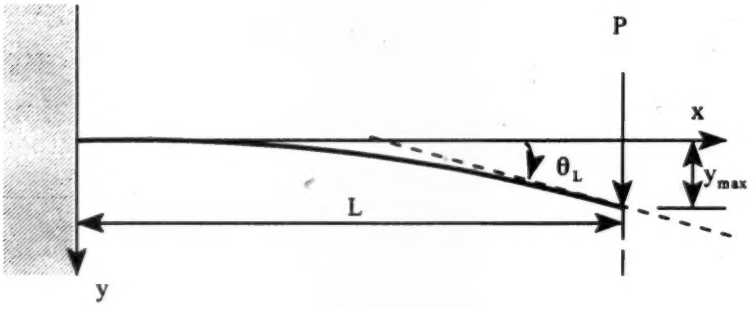


Figure 3.4 Single prismatic beam under concentrated force P

From a knowledge of mechanics, we know that a prismatic beam subjected to pure bending is bent into an arc of a circle and that, within the elastic range, the curvature of the neutral surface may be expressed as[32]:

$$\frac{1}{\rho} = \frac{M}{EI} \tag{3.2.1}$$

where ρ is the radius of curvature of the arc, M the bending moment, E the modulus of elasticity, and I the moment of inertia of the cross section about its neutral axis. However, both the bending moment and thus the curvature of the neutral surface will vary from section to section. Denoting by *x* the distance of the section from the (fixed) left end of the beam, we have

$$\begin{aligned} \frac{1}{\rho} &= \frac{M(x)}{EI} \\ &= \frac{P \cdot (L-x)}{EI} \end{aligned} \tag{3.2.2}$$

In which, $M(x) = P \cdot (L-x)$. See Figure 3.5 for reference.

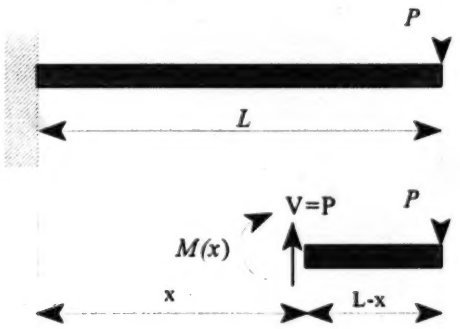


Figure 3.5 Free-body diagram of partial cantilever beam

Recall elementary calculus, the curvature of a plane curve at point (x, y) of the curve can be expressed as:

$$\frac{1}{\rho} = \frac{\frac{d^2y}{dx^2}}{[1+(\frac{dy}{dx})^2]^{\frac{3}{2}}} \qquad (3.2.3)$$

where dy/dx and d^2y/dx^2 are the first and second derivatives of the function $y(x)$. In the case of the elastic curve of a beam, the slope dy/dx is very small, and its square is negligible compared to unity. Therefore, we may write:

$$\frac{1}{\rho} = \frac{d^2y}{dx^2} \qquad (3.2.4)$$

Substituting for $1/\rho$ from (3.2.4) into (3.2.2), we have:

$$EI\ \frac{d^2y}{dx^2} = P\cdot(L-x) \qquad (3.2.5)$$

Integrating in x, we obtain:

$$EI\ \frac{dy}{dx} = -\frac{1}{2}Px^2 + PLx + C_1 \qquad (3.2.6)$$

At the fixed end we have $x = 0$ and $\theta = dy/dx = 0$ (see Figure 2.4). Substituting these values into the above equation, we have:

$$C_1 = 0$$

Equation (3.2.6) becomes:

$$EI\frac{dy}{dx} = -\frac{1}{2}Px^2 + PLx \tag{3.2.7}$$

Integrating equation (3.2.7), we write:

$$\begin{aligned} EIy &= -\frac{1}{6}Px^3 + \frac{1}{2}PLx^2 + C_2 \\ &= \frac{P}{6}(3Lx^2 - x^3) + C_2 \end{aligned} \tag{3.2.8}$$

At the fixed end of the cantilever, we have $y = 0$ when $x = 0$. Therefore, $C_2 = 0$. Thus, we obtain the equation describing the elastic curve of Figure 3.4:

$$y = \frac{P}{6EI}(3Lx^2 - x^3) \tag{3.2.9}$$

For the cantilever tip, the displacement is:

$$y_{max} = \frac{P}{6EI}(3Lx^2 - x^3)\Big|_{x=L} = \frac{PL^3}{3EI} \tag{3.2.10}$$

and the deflection angle is:

$$\theta_L = \frac{dy}{dx} = \frac{P}{2EI}(2Lx - x^2)\Big|_{x=L} = \frac{PL^2}{2EI} \tag{3.2.11}$$

Both equations (3.2.10) and (3.2.11) will be used later in the deflection calculation of CIC devices.

3.2.2 Deflection of a single cantilever beam under concentrated moment

Figure 3.6 shows a single cantilever beam under a concentrated moment M at the free end.

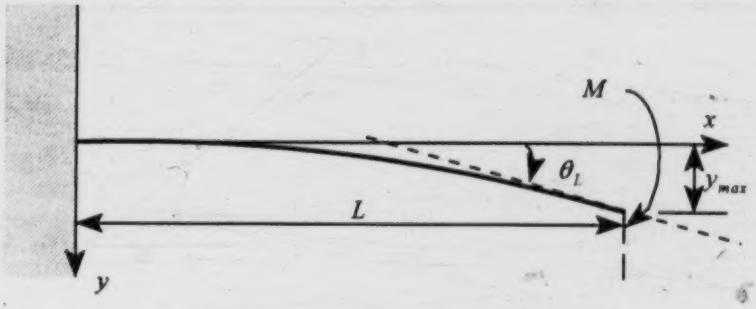


Figure 3.6 Single prismatic beam under concentrated moment M

Substituting (3.2.4) into (3.2.1), we have:

$$\frac{dy^2}{dx^2} = \frac{M}{EI} \tag{3.2.12}$$

Integrating in x, we obtain:

$$EI\frac{dy}{dx} = Mx + C_1 \tag{3.2.13}$$

At the fixed end we have $x = 0$ and $\theta = dy/dx = 0$ (see Figure 3.6). Substituting these values into the above equation, we have:

$$C_1 = 0$$

Using this result and integrating (3.2.13), we obtain:

$$EIy = \frac{1}{2}Mx^2 + C_2 \tag{3.2.14}$$

At the fixed end of the cantilever, we have $y = 0$ when $x = 0$. Therefore, $C_2 = 0$. Thus, we get the equation describing the elastic curve of Figure 3.6:

$$y = \frac{M}{2EI}x^2 \tag{3.2.15}$$

For the cantilever tip, the displacement is:

$$y_{max} = \frac{M}{2EI}x^2\Big|_{x=L} = \frac{ML^2}{2EI} \tag{3.2.16}$$

and the deflection angle is:

$$\theta = \frac{dy}{dx} = \frac{M}{EI}x\Big|_{x=L} = \frac{ML}{EI} \tag{3.2.17}$$

Both equation (3.2.16) and (3.2.17) will also be used in the following section to calculate the deflection of CIC devices.

3.2.3 Deflection of a triple cantilever-in-cantilever structure

The calculation of the deflection of a CIC structure discussed in this section follows the derivation given by B. Shen[33]. Figure 3.7 is the free-body diagram of the three cantilevers of a triple cantilever-in-cantilever structure. It should be noted that the direction of the y-axis is opposite to that used in Figure 3.5 and 3.6 for the convenience of calculation. For a cantilever with a small deflection, the system is linear. This means if the cantilever is under more than one load, the displacement and deflection are the algebraic sum of the results calculated under each load separately.

Corresponding to the side view of a triple cantilever-in-cantilever structure, Figures 3.7 (a), (b) and (c) represent the inner, intermediate and outer cantilevers separately. The inner cantilever is connected with the intermediate one at point A, while the intermediate and outer cantilevers are joined at point B. P_1, P_2 and P_3 represent the Lorentz forces exerted on the three ends of the structure. Assuming the external magnetic field intensity is uniform and parallel to the x-axis, P_1, P_2 and P_3 are parallel to the y-axis. For simplicity, P_1, P_2 and P_3 are approximated as concentrated forces. From experimental results, this approximation is valid (see section 3.3). M_1 denotes the moment acting at the A end of the intermediate cantilever with a magnitude of (P_1L_1) and M_2 denotes the moment acting at the free end of the outer cantilever with a magnitude of $[M_1 + (P_2-P_1)L_2]$. M_0 is the moment acting at the fixed end of the outer cantilever.

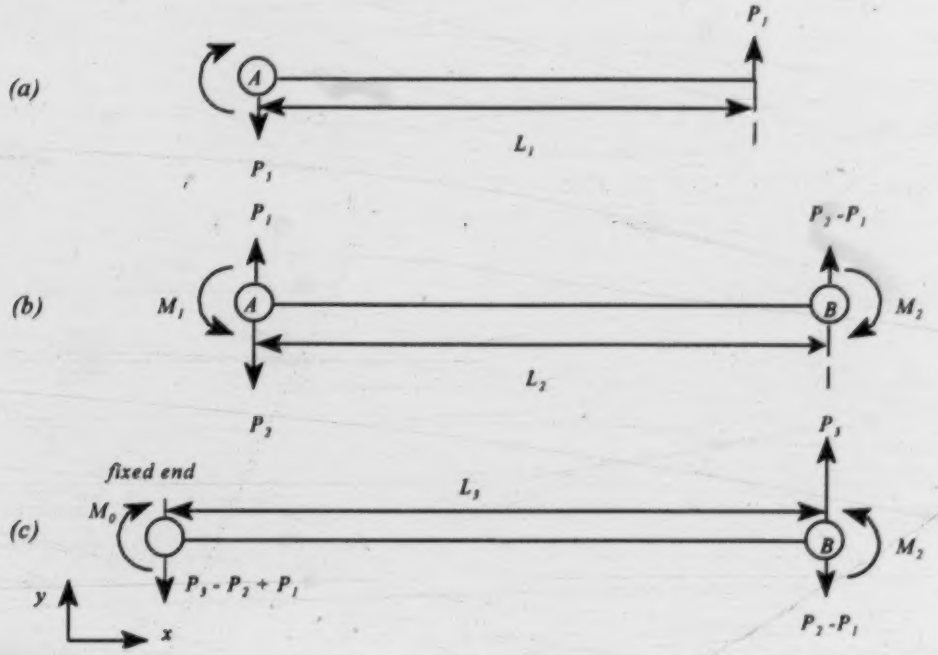


Figure 3.7 Free-body diagram of three cantilevers of a CIC structure

For the inner cantilever, there is a Lorentz force P_1 exerted on the right end of the cantilever. At point A, the reaction force and moment shown are required for static equilibrium. Considering the displacement y_1 and the deflection θ_{L1} of the inner cantilever with respect to point A, L_1 is substituted into equation (3.2.10) and (3.2.11). We have:

$$y_1 = \frac{P_1 L_1^3}{3EI}, \quad \theta_{L_1} = \frac{P_1 L_1^2}{2EI} \tag{3.2.18}$$

The displacement and deflection of the intermediate cantilever are more complex. At point A, the loading consists of Lorentz force P_2 along with the force and moment introduced by the inner cantilever. These forces and moment are also carried to the outer cantilever at point B (see Figure 3.7(c)). At point B, the reaction force and moment from the outer cantilever shown in Figure 3.7(b) are regarded for static equilibrium. The displacement and deflection of point A with respect to point B can be calculated from two aspects, the displacement and deflection introduced by the unbalanced force (P_2-P_1) and the displacement and deflection introduced by the moment $M_1 = P_1L_1$. Thus the total displacement and deflection of the intermediate cantilever can be calculated using equations (3.2.10), (3.2.16) and (3.2.11), (3.2.17):

$$y_2 = -\left[\frac{(P_2-P_1)L_2^3}{3EI} + \frac{P_1 L_1 L_2^2}{2EI}\right] \tag{3.2.19}$$

$$\theta_{L_1} = \frac{(P_2-P_1)L_2^2}{2EI} + \frac{P_1 L_1 L_2}{EI} \tag{3.2.20}$$

Similarly, the displacement and deflection of the outer cantilever can be calculated by substituting the unbalanced force (P_3 -(P_2 - P_1)) and the moment $M_2 = M_1+(P_2-P_1)L_2$ into equations (3.2.10), (3.2.16) and (3.2.11), (3.2.17):

$$y_3 = \frac{[P_3-(P_2-P_1)]L_3^3}{3EI} + \frac{[P_1L_1+(P_2-P_1)L_2]L_3^2}{2EI} \qquad (3.2.21)$$

$$\theta_{L_3} = \frac{[P_3-(P_2-P_1)]L_3^2}{2EI} + \frac{[P_1L_1+(P_2-P_1)L_2]L_3}{EI} \qquad (3.2.22)$$

Considering the central mirror plate of the CIC structure, its displacement and deflection are the accumulations of those of all the surrounding cantilevers when the deflection is relatively small. Written in a general form, the displacement and deflection of an nCIC structure (i.e. n cascaded cantilevers) are:

$$y_n = \frac{\sum_{i=1}^{n}(-1)^{i-1}F_iL_i^3}{3EI} + \frac{\sum_{i=1}^{n-1}(-1)^iM_iL_{i-1}^2}{2EI}$$

$$\theta_{L_n} = \frac{\sum_{i=1}^{n}F_iL_i^2}{2EI} + \frac{\sum_{i=1}^{n-1}M_iL_{i-1}}{EI} \qquad (3.2.23)$$

in which,

$$F_1 = P_1;$$

$$F_i = P_i - F_{i-1} \quad (i>1);$$

$$M_i = \sum_{j=1}^{i}F_jL_j$$

Since the displacements of two successive cantilever ends are always in opposite directions, a partial cancellation of the displacement of the central mirror plate occurs. However, since the θ_i have same sign, all the cantilevers contribute to the accumulation of

deflection in the same direction. Thus, triple CIC structures may have large deflection angles when the displacement is small. It improves the deflection magnitude over the simple cantilever structure under the same operating conditions. In Sec. 3.3, deflections of cantilever structures from a single one to the nCIC are compared, and the results show that the static deflection angle of a triple CIC structure is more than ten times of that of a single cantilever.

Moreover, we may also predict that the total deflection is proportional to the Lorentz forces and therefore to the external magnetic field B and the input current I_e.

3.2.4 Limitation of deflection calculation

From equation (3.2.23), we may conclude that the more embedded cantilevers there are, the more the attainable angular deflection due to the effect of the deflection accumulation. But is equation (3.2.23) always suitable? Or in other words, what is the limitation of equation (3.2.23)?

During the above derivation, equation (3.2.4) is used in the calculation of single cantilever deflection under both concentrated force and concentrated moment. It should be noted that equation (3.2.4) came from equation (3.2.3) with assumption that $d^2y/dx^2 \ll 1$. Since $\tan\theta = dy/dx$, the limitation of equation (3.2.23) is $\tan^2\theta \ll 1$. Taking $\tan^2\theta \leq 0.1$, we have $\theta \leq 17.5°$. So equation (3.2.23) is suitable only when the deflection of every cascaded cantilever is smaller than 17.5°. Experimental results and theoretical estimation of the static deflection of the CIC devices discussed in the following sections are all obtained within this limitation, i.e. the deflection of every cantilever is smaller than 17.5°.

In the next two sections of this chapter and the next chapter, these theoretical results will be verified by experiment and simulation.

3.3 Experiments and Analyses

A series of cantilever-in-cantilever structures have been designed and fabricated to test the theoretical prediction of deflection. Figure 3.8 is a SEM picture of a group of cantilevers from a single cantilever to a quadruple cantilever.

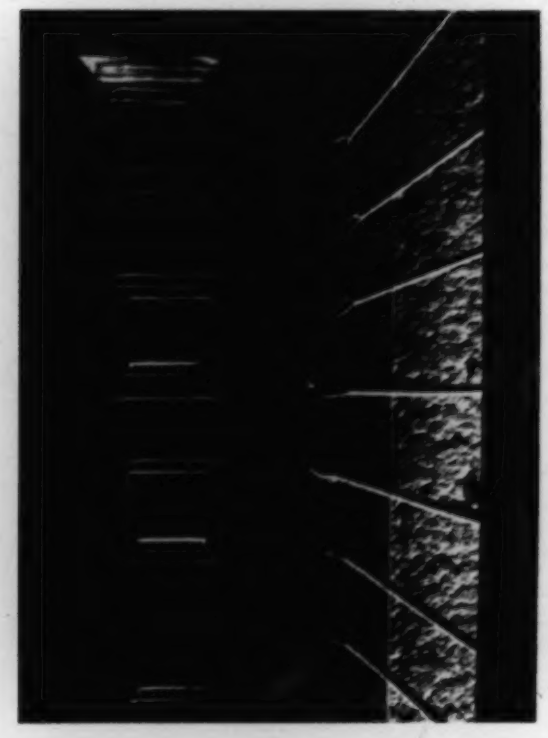


Figure 3.8 SEM picture of a group of cantilevers

The series of cantilever structures was built using the standard CMOS 1.5 micron process offered by Mitel. The anisotropic etching was performed at the Alberta Microelectronic Centre (AMC). For these cantilevers, the dimensions in microns are:

$$l_1 = 250, \quad l_i = 285 + 70\times(i-2) \qquad 2\le i\le n, \quad n\le 4$$

$$L_1 = 205, \quad L_i = 240 + (i-2)\times 55 \qquad 2\le i<n, \quad L_n = 260 + (n-2)\times 55 \quad n\le 4$$

in which l represents the length of the wire perpendicular to the external magnetic field and L represents the length of the supporting arms. The subscript indicates the corresponding cantilever, going from the inner to the outer one. For example, L_n stands for the length of the longest supporting arm.

3.3.1 Experimental set-up and optical detection method

The deflection of the cantilever is measured by an optical method. Figure 3.9 is the experimental set-up for the deflection measurement.

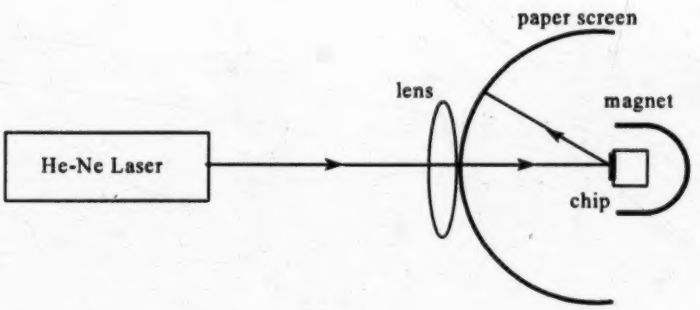


Figure 3.9 Experimental set-up for the deflection measurement

The beam coming from the helium-neon laser (Spectra Physics, Model 155) is focused on the mirror plate of the cantilever structure on the chip. The deflection of the mirror plate can be measured by measuring the position of the reflected light spot on the paper screen (see Figure 3.10). The paper screen is a semi-circle containing graduations on the inner surface. The radius of the screen is equal to the focal length of the lens. Thus, the deflection angle can be easily read out on the paper screen. From Figure 3.10, we can see:

$$\chi + 2\alpha + 2(90^\circ - \alpha - \theta) = 180$$
$$\chi = 2\theta \qquad (3.3.1)$$

in which χ is the angle measured on the paper screen, α is the angle of incidence and of reflection when the mirror plate is at rest. θ is the deflection angle of the mirror plate.

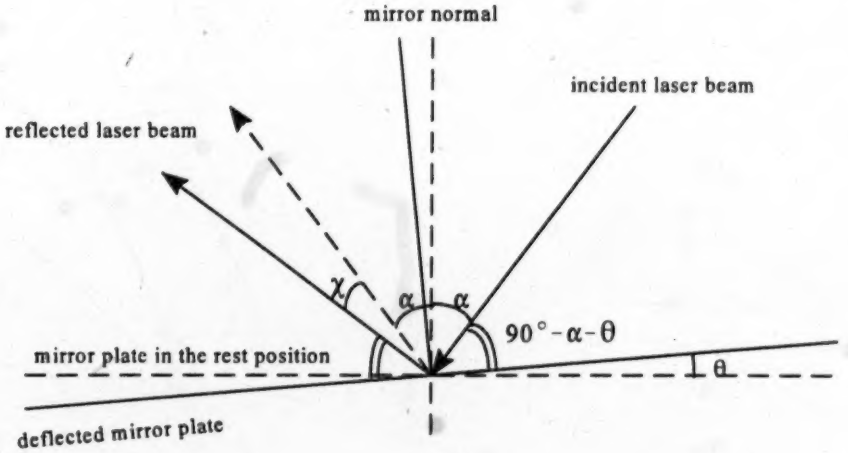


Figure 3.10 Deflection angle illustration

3.3.2 Parameters for the deflection calculation

To calculate the deflection of the cantilever-in-cantilever structure, the mechanical properties of the suspension arms, such as Young's modulus and density of the different CMOS-compatible materials are approximated with the corresponding bulk values, as given in Table 3.1. We use bulk values because values pertaining to thin films are generally not available. The thickness of every layer is needed to calculate the centroidal moment of inertia I.

Table 3.1 Mechanical properties of CMOS thin film materials

Material	Young's Modulus (Gpa)	Density(kg/m^3)
Aluminum	*72*	2.7×10^3
Polysilicon	*168*	2.3×10^3
Silicon Dioxide	*74*	2.2×10^3
Silicon Nitride	*320*	2.8×10^3

3.3.2.1 *Layer thicknesses*

Figure 3.11 illustrates the thickness profile, obtained from the CMOS 1.5 μm process data provided by Mitel[34]. A process outline is also given in reference [18]. A detailed layout diagram of a triple cantilever-in-cantilever structure is given in Figure 3.3.

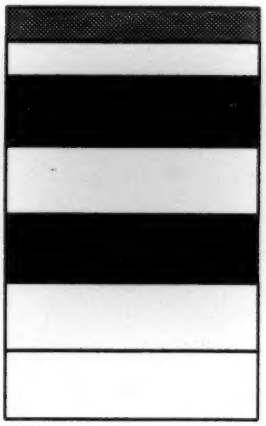


Figure 3.11 Layer thickness of Mitel 1.5 μm micromachined structure

3.3.2.2 Calculation of centroidal moment of inertia

Figure 3.12 is the cross section of a typical cantilever support arm with one metal layer embedded. All layers of silicon dioxide, including the dielectric deposition, inter-dielectric, spin-on-glass and passivation oxide layer, are merged together.

Young's modulus E is similar for the silicon dioxide and the aluminum (see Table 3.1), so the oxide and the aluminum can be regarded as a homogeneous material (see Figure 3.12(a)). In order to calculate the centroidal moment of inertia, the rectangular shape of the cross section, which now contains two different materials, oxide and nitride, can be transformed into a T-shaped cross section with the same Young's modulus as the oxide portion by scaling the width of the nitride layer by a factor of r, which is the ratio of the elastic modulus of nitride to oxide (see Figure 3.12(b)):

$$r = \frac{E_{nitride}}{E_{oxide}} = 4.324 \qquad (3.3.2)$$

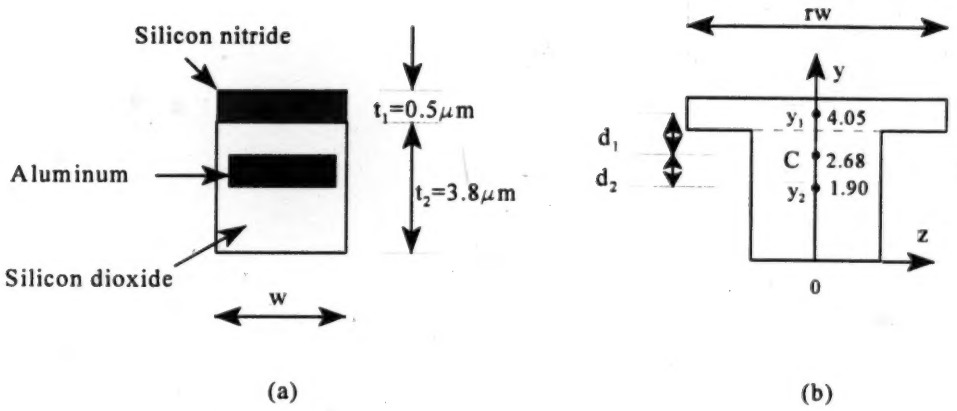


Figure 3.12 Cross section of a typical supporting arm of a cantilever structure

First, we have to locate the centroid C. We divide the T-shaped cross section into the two rectangles shown and write:

$$\bar{Y} \Sigma A = \Sigma \bar{y} A \qquad (3.3.3)$$

in which Y is the coordinate of centroid C and y is the coordinate of the centroid of each rectangle separately; A denotes the area of each rectangle. Therefore, we have:

$$\bar{Y} = \frac{\sum \bar{y} A}{\sum A} = \frac{\bar{y}_1 \times rw \times t_1 + \bar{y}_2 \times w \times t_2}{rw \times t_1 + w \times t_2}$$

$$= \frac{(4.05 \times 0.5 \times 4.324 + 1.9 \times 3.8) \times w}{(4.324 \times 0.5 + 3.8) \times w}$$

$$= 2.67965\,(\mu m) \qquad (3.3.4)$$

The parallel-axis theorem is then used to determine the moment of inertia of each rectangle with respect to the axis which passes through the centroid of the composite section. Adding the moments of inertia of the rectangles, we have:

$$I = \sum (\bar{I} + Ad^2) = \bar{I}_1 + A_1 d_1^2 + \bar{I}_2 + A_2 d_2^2$$

$$= \frac{1}{12}(4.324 \times w) \times 0.5^3 + (4.324 \times w) \times 0.5 \times 1.37035^2$$

$$+ \frac{1}{12} w \times 3.8^3 + w \times 3.8 \times 0.77965^2$$

$$= 10.9875w \ (\mu m^4) \qquad (3.3.5)$$

in which w is the width of the supporting arms. For all the CIC structures discussed in this thesis, w is 15 μm.

3.3.2.3 External magnetic field

The external magnetic field is produced from a horseshoe permanent magnet. The magnetic field was measured using a Gauss meter (Radio Frequency Laboratories, Inc., Boonton, New Jersey, U. S. A, Model 1890). Figure 3.13 is the conceptual diagram for the region which has a uniform magnetic field. Within the central volume of 5 mm × 5 mm × 6 mm, the magnetic field is relatively uniform with a value of 0.14 T. The relative variation is about 2%.

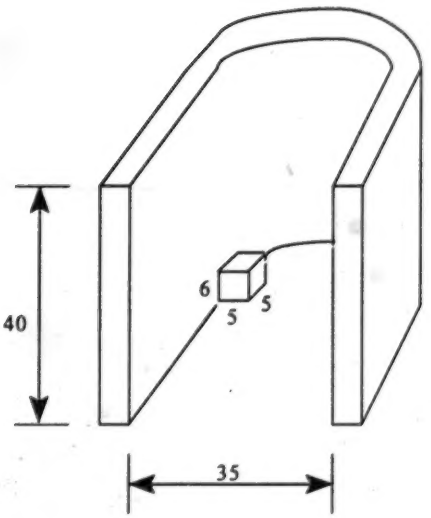


Figure 3.13 Conceptual diagram of the region with uniform magnetic field. Dimensions are in mm.

3.3.3 Comparison of the theoretical calculation with experiment results

After we obtain all the necessary parameters, equation (3.2.23) can be used to calculate the deflection of the series of cantilever structures. Splus, a programming language which is commonly used in statistics, was used to write a code to calculate deflection of a series of CIC structures from a single cantilever to a quadruple, using equation (3.2.23). The Splus program is listed in Appendix A. Figure 3.14 compares the theoretical calculation with experiment results.

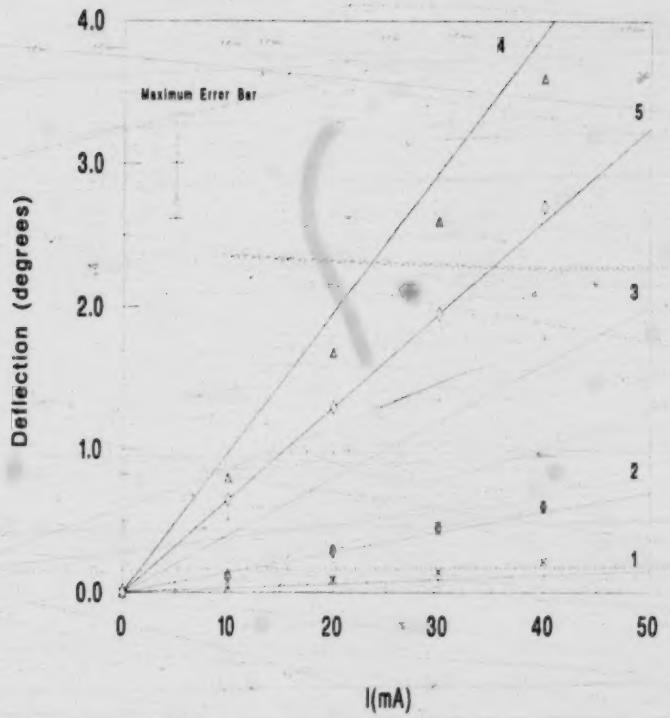


Figure 3.14 Deflection of a series of CIC structures

Both analytic estimates and experimental results of the cantilevers' deflections from a single to a quadruple are shown in the figure. Lines 1 to 4 correspond to the analytic estimations of cantilevers from single to quadruple. Line 5 corresponds to the analytic estimation of a triple CIC without the field oxide layer. All the analytic estimation lines are drawn from the results of the Splus program (see Appendix A).

Experimental results are plotted by different symbols in Figure 3.14. The experimental set-up and optical detection method are introduced in Sec. 3.3.1. All the experiment data have been treated by subtracting the thermal deflection at each current. Within the permitted range of error, all the experimental results can be regarded as linear with respect to the currents as predicted by the calculation in Sec. 3.2.

The error of experimental results mainly comes from the reading of the deflection on the paper screen. Curving of the mirror plate due to inherent stress often occurs after releasing the structure by wet anisotropic etching. The reflected light spot of the mirror plate on the paper screen is about 2.0 cm × 1.5 cm because of divergence caused by this curvature. The maximum reading error is about 2 mm, which is equal to 0.358° of the mirror deflection.

In Figure 3.14, the experimental deflections of single, double and triple cantilevers are all larger than the corresponding analytically calculated deflections. We think this systematic error comes from the inaccurate thickness used in the analytic calculation. The layer thickness profile is obtained from the CMOS 1.5 μm process data provided by Mitel, but the actual thickness may be different from the manufacturer's specified value. A SEM picture of a sliced Mitel chip is shown in Figure 3.15. The picture is not very clear and there is an angle for observation, which makes it difficult to obtain the exact thickness of every layer, but it shows that the actual thickness is smaller than the standard values given by Mitel. Some design rules have to be violated in order to fabricate the mechanical structures in the micromachining design. In doing so, some of the layers may be attacked by subsequent processing steps and thus the thickness of some layers may be changed. Also, anisotropic etching decreases the dimension of the structures. In combination of all the above reasons, the deflection of the real structure is larger than the analytic calculation because of the decreased thickness and thus decreased centroidal moment of inertia.

The quadruple CIC device also has the thickness problem mentioned above, but the chip is not completely etched. Silicon dioxide residue was found between supporting arms, especially near the webs of two successive cantilevers, which decreases the effective length of the supporting arms. Therefore, a decreased deflection was obtained.

Curve 5 corresponds to a triple CIC device without field oxide, so the beams are

about 0.7 μm thinner than the other devices. The corresponding moment of inertia is 6.68w (μm^4). This device is fabricated by a different run, and the better fit would indicate that the thickness is close to the given value.

Figure 3.15 SEM picture of a sliced Mitel chip

Figure 3.16 displays the total deflection of another triple CIC device as a function of both AC and DC current. The total deflection of the DC current actuation represents the total angular displacement up and down. It is obtained by reversing the DC current. The frequency of the AC current is 100 Hz, and the current measured is the rms value. The deflection for both AC and DC are linear with respect to the current as predicted by the analytic calculation. The experimental results are fitted by straight lines. The slope of AC actuation is about $\sqrt{2}$ times that of DC actuation, which is explained by the relationship between peak value and average value of the AC current.

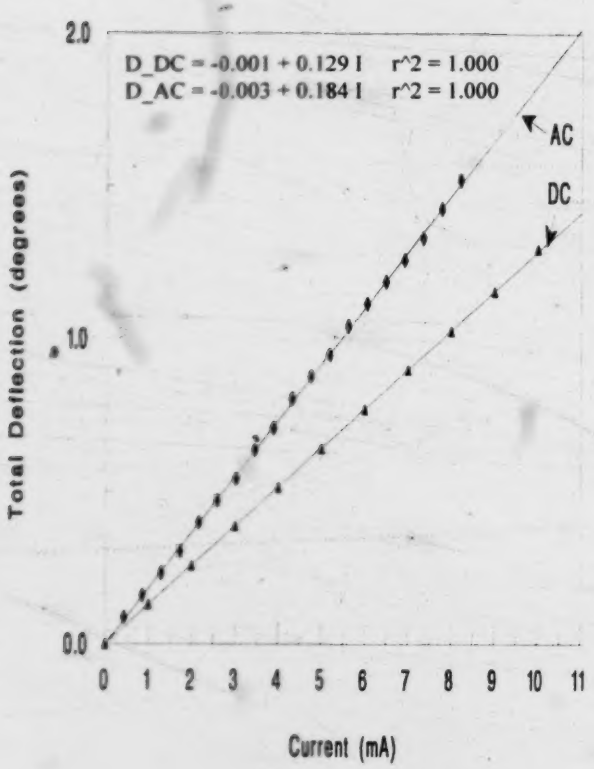


Figure 3.16 Total deflection variation with AC and DC current

Conclusion:

A series of CIC devices has been designed and tested. The results shown in this section indicate that the analytic calculations of the static deflections predicted in Sec. 3.2 are acceptable.

3.4 Resonant Response

The resonant response is an important factor of the CIC device. There are some important applications of the device making use of the resonant response. Resonant response of a triple CIC device is discussed in this section. Potential applications of the devices will make use of the resonant response, as indicated in Sec. 3.6.

3.4.1 Uncoupled flexural equations of damped motion

The resonant vibration of the CIC structure might be described using the classical equations of linear elasticity[35]:

$$\rho\frac{\partial^2 z}{\partial t^2} + \rho_1\frac{\partial z}{\partial t} + Lz = q(x,y,z) \tag{3.4.1}$$

in which,

$$\begin{aligned} L(z) = {} & \frac{\partial^2}{\partial x^2}[D_x\frac{\partial^2 z}{\partial x^2}] + \frac{\partial^2}{\partial y^2}[D_y\frac{\partial^2 z}{\partial y^2}] + \\ & \frac{\partial^2}{\partial x^2}[D_1\frac{\partial^2 z}{\partial y^2}] + \frac{\partial^2}{\partial y^2}[D_1\frac{\partial^2 z}{\partial x^2}] + 2\frac{\partial^2}{\partial x\partial y}[D_{xy}\frac{\partial^2 z}{\partial x\partial y}] \end{aligned} \tag{3.4.2}$$

denotes the stiffness of the device, and D_x, D_y, D_1 and D_{xy} are called the flexural rigidities, ρ the area density, ρ_1 the damping term and q the load. Detailed dynamic numerical simulation of CIC structures is given in reference [35], and an ANSYS simulation of the resonance is included in Chapter 4.

3.4.2 Experiment results

To obtain the resonant response of the CIC devices, a sine wave AC current is applied

to actuate the device by a Hewlett Packard 15 MHz function/arbitrary waveform generator (model 33120A). Figure 3.17 is the resonant response of a triple CIC structure without the field oxide layer. The total deflection is measured using the optical method introduced in Sec. 3.3.1 at a current of 3 mA and 10 mA separately. No lateral oscillations, mentioned in reference [33], have been found, due, we believe, to the geometric symmetry of the structure. Experimental results are fitted by the interpolation method of CA-Cricket Graph ™ version 1.3.1(©1991 Microsoft Corporation). The interpolation method uses regression to formulate the curve.

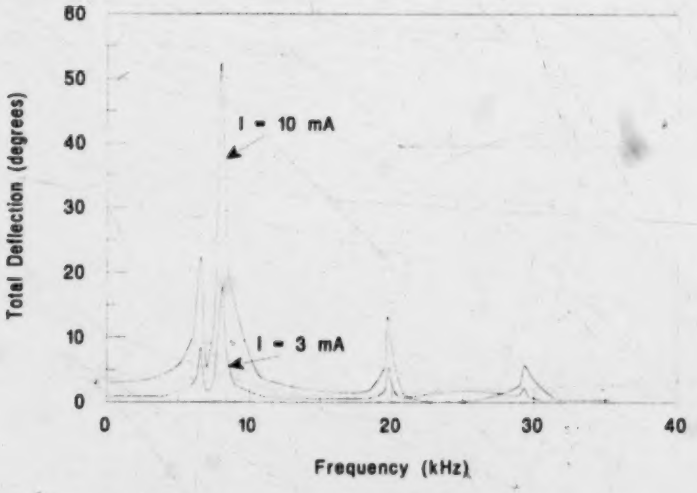


Figure 3.17 Resonant response of a triple CIC structure without the field oxide layer

The damping ratio is an important parameter for a real vibration system. It affects the shape of the deflection curve near resonance. From the above experimental results, the damping ratio of the system may also be obtained using the bandwidth (half-power) method[32]. Since the shape of the entire frequency-response wave is controlled by the amount of damping in the system, it is possible to derive the damping ratio from the properties of the curve. The bandwidth method is one of the most convenient methods. The damping ratio is

determined by the frequencies at the half-power point at which the response is reduced to $1/\sqrt{2}$ of its maximum value.

Figure 3.18 shows details of the calculation of the damping ratio. First, the peak response is determined to be 52.5° from experimental results. Then at peak $\div\sqrt{2}$= 37.12° determine the two frequencies of the response curve: f_1= 7.78 kHz, f_2= 8.25 kHz. Finally, the damping ratio ξ is given by:

$$\xi = \frac{f_2 - f_1}{f_2 + f_1} = 2.93\% \qquad (3.4.3)$$

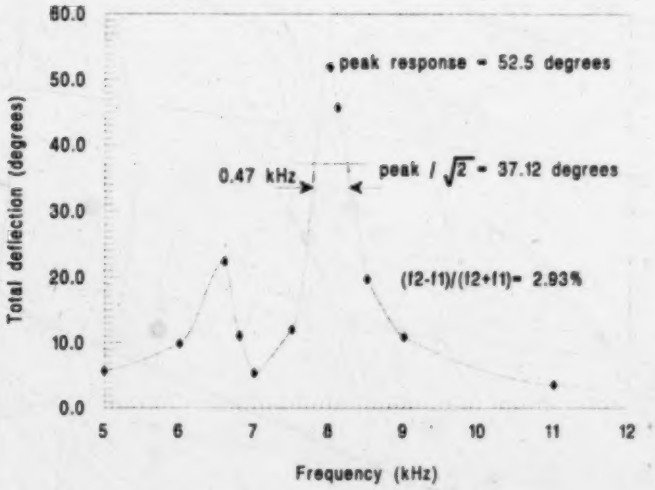


Figure 3.18 Frequency-response experiment to determine damping ratio

The relationship between damping ratio ξ and the damping term ρ_1 in equation (3.4.1) is[32]:

$$\xi = \frac{\rho_1}{2\omega\rho} \qquad (3.4.4)$$

Since the experimental curve is fitted by an interpolation method, flexible splines are used to connect sparse experimental points. We can also use a general function to represent resonance with damping, given by:

$$D = \frac{A\gamma}{(f_0 - f)^2 + \gamma^2/4} \tag{3.4.5}$$

in which D represents the deflection, f is frequency and f_0 is the resonant frequency, and γ is a damping term. Equation (3.4.5) is fitted to the experimental data using a least-squares method (see Figure 3.19). The fit is best for A= 8.875 kHz· degree and γ= 0.7 kHz. γ and ξ are linear related, that is $\gamma = k\xi$. For the CIC device around 8.0 kHz, k≈23.6 kHz.

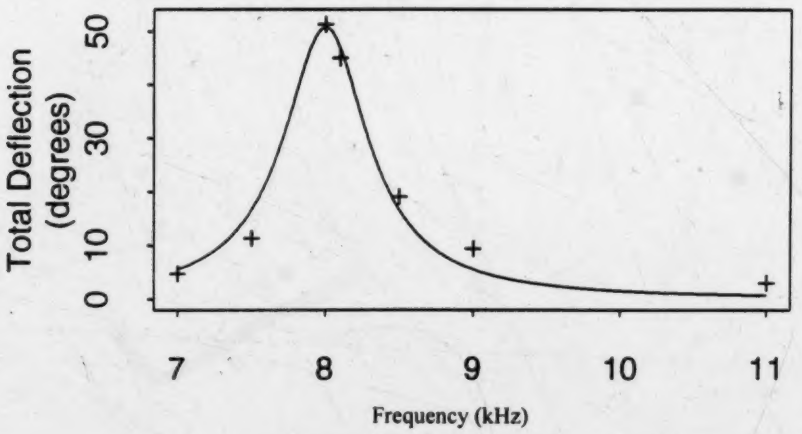


Figure 3.19 Deflection curve near resonance

3.4.3 Resonant frequency versus input current

The resonant frequencies of the CIC structures have been measured under different input current. Figure 3.20 shows the deflection curves near resonant frequencies 6.6 kHz and 8.1 kHz. The deflection is measured using the optical method and curves 1 to 4 correspond to the input current I_1=3 mA, I_2=10 mA, I_3=20 mA and I_4=25 mA. The first resonant

frequency (6.6 kHz) has no obvious change during the experiment. The second resonant frequency decreases with the input current from 8.17 kHz at 3 mA, decreasing to 8.08 kHz at 25 mA (8.13 kHz at 10 mA and 8.09 kHz at 20 mA).

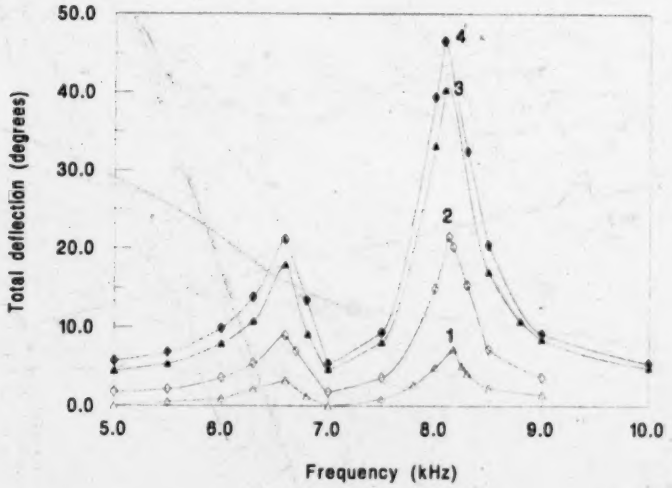


Figure 3.20 Resonant frequency changing versus input current

The shift of resonant frequency is due to the variation of temperature of the supporting arms. The increased input current increases the average temperature of not only the aluminum but of all the materials, which may change the inherent stresses and stiffness of the structure and thus change the resonant frequency. Figure 3.21 is the resonant frequency variation curve versus the temperature increase of the supporting arm. The temperature increase of the arm is measured by measuring the resistance change of the aluminum lead at each current. Details about the temperature measurement are discussed in Sec. 3.5.2.

The experimental results in Figure 3.21 are fitted using a polynomial. For the CIC devices tested here the maximum variation is approximately 0.003 kHz/°C. Consequently,

the resonant frequency variation with temperature should be considered in some applications of CIC devices as a resonant sensor.

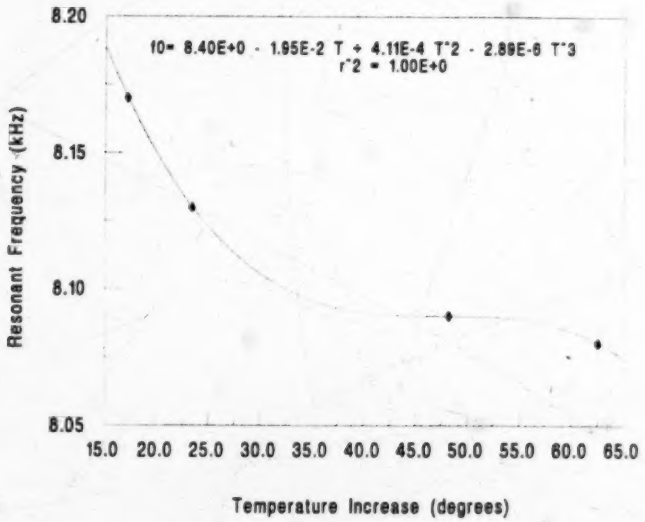


Figure 3.21 Resonant frequency variation versus temperature increase

3.4.4 Lifetime testing of the CIC devices

The triple CIC device has been operated at resonance (about 8.2 kHz) at an AC current (I_{rms} ≐ 5 mA) continuously for 55 days and 10 hours (about 3.9×10^{10} oscillations). Total deflection is about 25° and the maximum displacement of the central mirror plate is about 50 μm. No visible deflection change and resonant frequency shift was observed afterward.

The stability of the resonant response and characteristics of the CIC devices provides the base for the potential applications of the CIC structures as resonant sensors and actuators, which is discussed in Sec. 3.6.

3.5 Thermal Effects on the CIC Structure

Thermal effects acting on the cantilever-in-cantilever structure also contribute to the deflection when the Lorentz force arising from the interaction between the currents flowing in the cantilever and an external magnetic field is used to actuate the structure. This comes from Joule heating in the metal leads. In this section, the thermal actuation will be discussed and a temperature cooling phenomenon will also be explained.

3.5.1 Thermal actuation

Electro-thermal actuation is also an important feature in sensor technology[36-38]. The actuation occurs when two layers of different materials with different coefficients of thermal expansion are attached and subjected to a temperature increase; a mechanical deflection towards the material with the lower thermal expansion coefficient will occur. For the CIC structure introduced in the last several sections, Joule heating on the periphery of the structure is discussed in this section.

Figure 3.22 shows the result of a thermal effect measurement. Three curves are shown in Figure 3.22. Curve 1 is for a DC current that produces a deflection of the central cantilever up out of the plane of the substrate; Curve 3 is obtained with current in the opposite direction and which produces a deflection down below the plane of the substrate. Curve 2 corresponds to the current in either direction, but with no magnetic field. The deflection is essentially the same for either direction, and is produced by the thermal effect only.

The flat portion of curve 3 in Figure 3.22 indicates an incompletely etched pillar of silicon underneath the structure, preventing further deflection (see section 2.4.1). When the applied current is more than 20 mA, the mirror plate hits the unetched silicon pillar and the deflection remains constant when the input current increases.

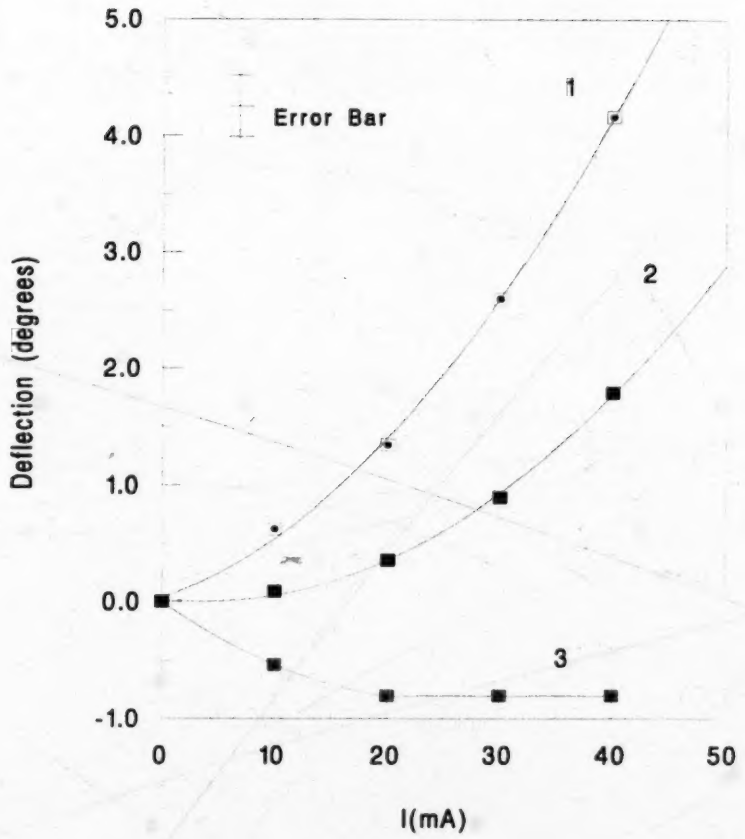


Figure 3.22 Thermal effect of a triple CIC actuation

To eliminate the thermal effect, the values of average thermal deflection as plotted by curve 2 are subtracted from the corresponding values of curves 1 and 3. Figure 3.23 is the deflection without thermal effects. The data are least-squares fitted to straight lines, while the two data points obtained when hitting the unetched pillar are not considered during curve fitting. They are marked by different symbols in Figure 3.23.

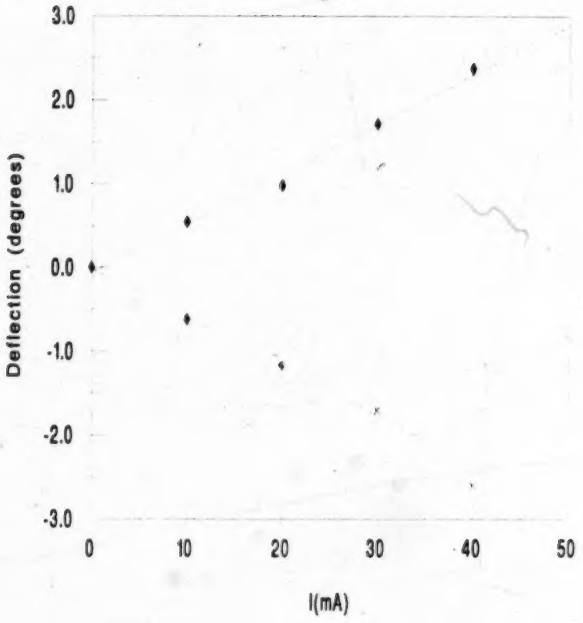


Figure 3.23 Deflection of a triple CIC structure without thermal effects

The deflections plotted in Figure 3.23 are linear to the input current as predicted by the analytic estimation.

Usually during experiments we eliminate the thermal effect by reversing the direction of the current and measuring the total deflection of the device. For DC input current, the measurement on the two reflected beam positions produced by the same current flowing in opposite directions is used to determine the cantilever deflection. Thus, the results shown in Figure 3.24 are obtained from Figure 3.23 by subtracting the negative deflections from the positive ones. For AC input current, the reflected beam scans on the screen with the input

current frequency and forms a ribbon of light. Total deflection is obtained by the measurement on the two edges of the light ribbon and then subtracting the original size of the reflection spot (usually about 2.0 cm).

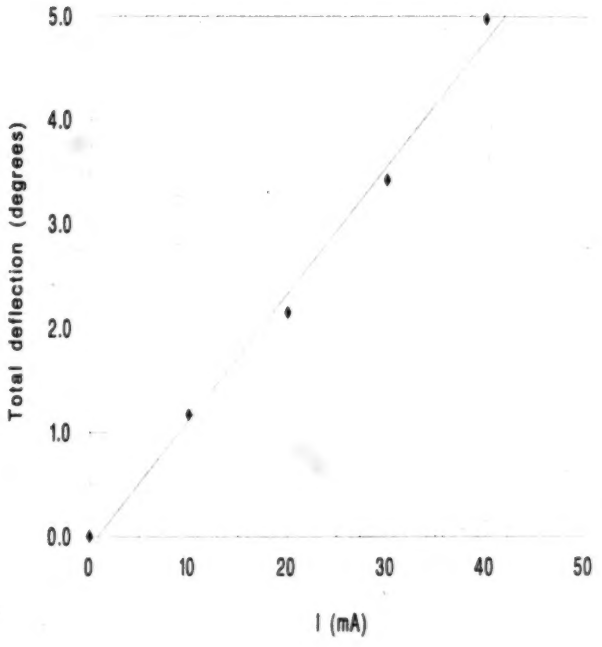


Figure 3.24 Total deflection of a triple CIC structure

3.5.2 Temperature effect at resonance

The average temperature of the support arms of CIC structures can be measured using the aluminum lead as a temperature sensing element. As we know:

$$R(T) = R_0[1 + \alpha(T - T_0)] \tag{3.5.1}$$

Here R(T) is resistance at temperature T, R_0 is resistance at a reference temperature T_0, and α is the temperature coefficient of resistance (TCR) of Aluminum. Thus, we have:

$$T = T_0 + \frac{R(T) - R_0}{\alpha R_0} \tag{3.5.2}$$

The resistance of aluminum is measured by measuring both voltage across the aluminum and the current flowing through it.

When we measured the temperature of the supporting arms around the resonant frequencies of the CIC structures, an interesting cooling phenomenon was observed. When the device was driven through resonance by an AC sine wave current of 10 mA at atmospheric pressure, there is about a 0.5°C dip in the average temperature at resonance. Figure 3.25 shows the temperature dip of two identical CIC devices but on different chips. The first two resonant frequencies of the two devices are 6.6 kHz, 8.2 kHz and 6.6 kHz, 8.4 kHz. Experimental data are joined by interpolation.

It is proposed that at resonance, the center plate acts like a mechanical fan due to the large magnitude of its deflection and it pushes the ambient air much faster, cooling the device. If the above hypothesis is correct, then there will be no dip in the average temperature of the support arms when the whole experiment is performed in a vacuum. Such an experiment has been done and is discussed below.

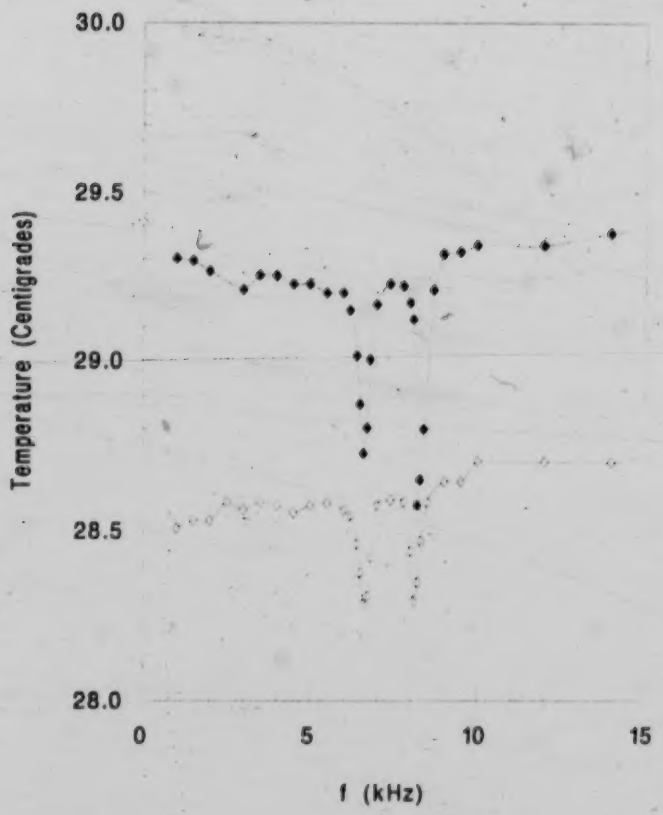


Figure 3.25 Temperature increase of the support arms versus driving frequency

3.5.2.1 High vacuum testing system

Figure 3.26 is the conceptual diagram of the high vacuum system, which is a diffusion pumped vacuum system. A bell jar is used to house the equipment.

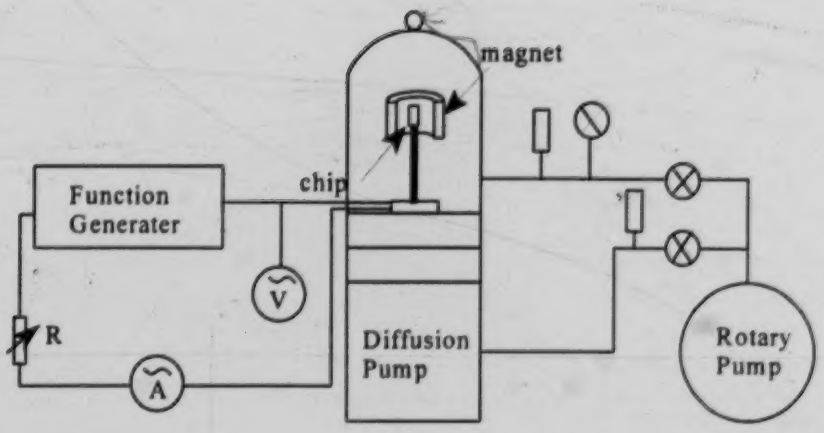


Figure 3.26 Conceptual diagram of the vacuum system

3.5.2.2 Experimental results

The average temperature of the support arms has been measured in the vacuum system under pressure of 700 Torr and 2×10^{-5} Torr separately. Figure 3.27 shows the experimental results. It should be noted that the temperature values of the second curve (p = 2×10^{-5} Torr) have been reduced by 110°C to fit the two curves into the diagram. The input current is about 10 mA. It heats the support arms to a much higher temperature in the vacuum since the heat transfer through ambient air has been effectively eliminated at 2×10^{-5} Torr.

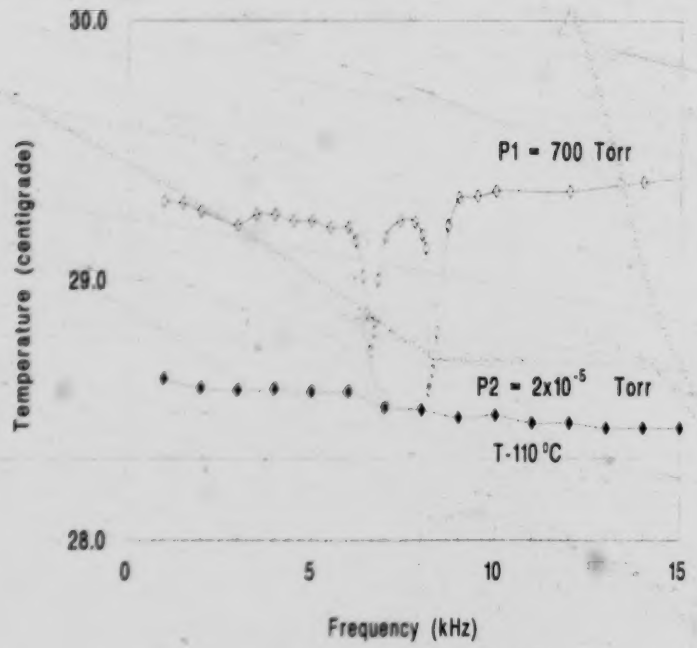


Figure 3.27 Temperature variation under atmospheric pressure and $2x10^{-5}$ Torr

Voltages across and currents flowing through the CIC device are measured every 1.0 kHz under the vacuum and recorded by hand. Observations between those measured data points were made and no resonant dip was seen. Thus, experiment shows that no temperature dip has been found at resonance under vacuum, which supports the hypothesis that the large oscillation of the central cantilever in air cools the structure.

3.6 Applications of the CIC Device

By making use of the resonance vibration feature and large spread angle characteristics of the structure, the CIC devices have many potential applications, such as:

• Resonator Sensors (including temperature sensors and chemical sensors making use of resonance characteristics): The resonant frequency of the structure is sensitive to a variety of measurands, such as the temperature and the mass of the structure. Therefore, the CIC structure can be designed as a temperature sensor or a chemical sensor. When a thin layer of material which can absorb gases or vapor, for instance, is deposited on the surface of the structure, the change of the mass can be detected by the shift of resonant frequency.

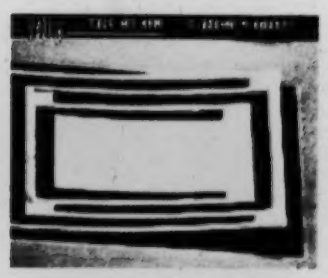
• Optical Choppers: The vibration of the CIC structures may be used as an optical chopper. Combining the advantages of micromachining with optical fibre techniques, optical sensors may lead to new developments in optical communication devices.

• Material property extraction: The performance of the CIC devices depends on the parameters of the materials forming the structure. Thus, from the performance of the structure, some material properties may be extracted.

• Image System: The CIC devices may be fabricated as a array. The mirror plates of the CIC devices can be used to reflect incident light with separate actuations. Thus, an image composed of the reflected light spots can be produced.

The above are four preliminary predictions. There are many other possible applications. The device needs optimization, however, and the feasibility of magnetic actuation for some of the applications needs further investigation.

4



ANSYS Simulation

The finite element method is a powerful approach for analyzing physical problems for which no closed-form analytical solutions exist. ANSYS, a commercial finite element package available from Swanson Software is used extensively in Civil and Mechanical Engineering as an analysis tool for such things as frames and structures, plates and shells, vibration, acoustics and heat transfer. In this section, two updated versions, ANSYS 5.2 and 5.3, were used to simulate the resonant vibration of the CIC structures. The ultimate purpose is to optimize the structure performance from the results of simulation.

Generally, the whole process of simulation is divided into three distinct steps. The first step is building the model. The choice of a suitable element type is a key step in obtaining satisfactory simulation results. In this step, the type of element, the real constants of the element and the material properties are defined. The second step involves applying loads and obtaining solutions. The loads include boundary conditions (constraints, supports, or boundary field specifications) as well as other externally and internally applied loads. The

last step is reviewing the results. Once the solution has been calculated, the ANSYS post-processors are used to review the results. Contour displays, deformed shapes, and tabular listings and graph plots etc., can be obtained, to review and interpret the results. Figure 4.1 shows a model built for a three-dimensional single cantilever device that has been etched to free it, along with the anisotropic etching pit. In the following analysis, only the released device part is simulated for the purpose of simplicity.

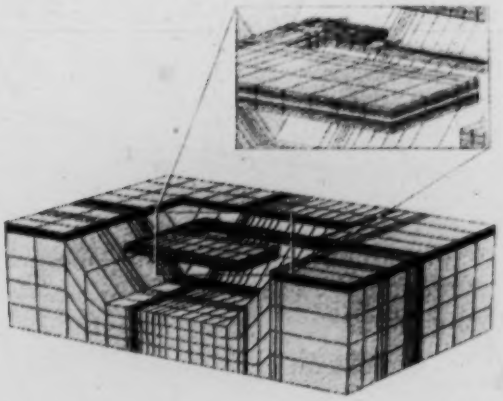


Figure 4.1 Three-dimensional model built for cantilever structure

The ANSYS program has many finite element analytical capabilities. In the next two sections, static deflection characteristics of the CIC structures will be simulated using a linear static analysis method. The resonant vibration of the structures will be simulated using the dynamic modal analysis.

4.1 Linear Static Analysis

A triple CIC structure fabricated by the Nortel CMOS4S process has been simulated using ANSYS 5.2. The structure has the same design scale dimension as Figure 2.2, but the real device has a 20% shrinkage because of the Nortel process. The ANSYS simulation code is given in Appendix B.

Since there is a plane of symmetry of the CIC structure, only half of the structure is analyzed to cut down on the computational time required to solve the system's unknowns. Figure 4.2 shows the deformed shape of the half CIC structure and Figure 4.3 shows the deflection detail from the side view, for current I_e = 10 mA and B = 0.14 T. It should be noted that the scales on different axes are different and the coordinates are different from the previous ones used in Sec. 3.2.

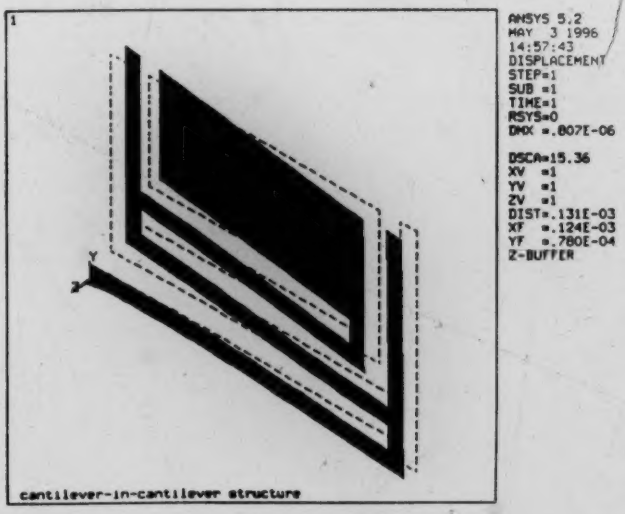


Figure 4.2 Deformed shape of a CIC structure

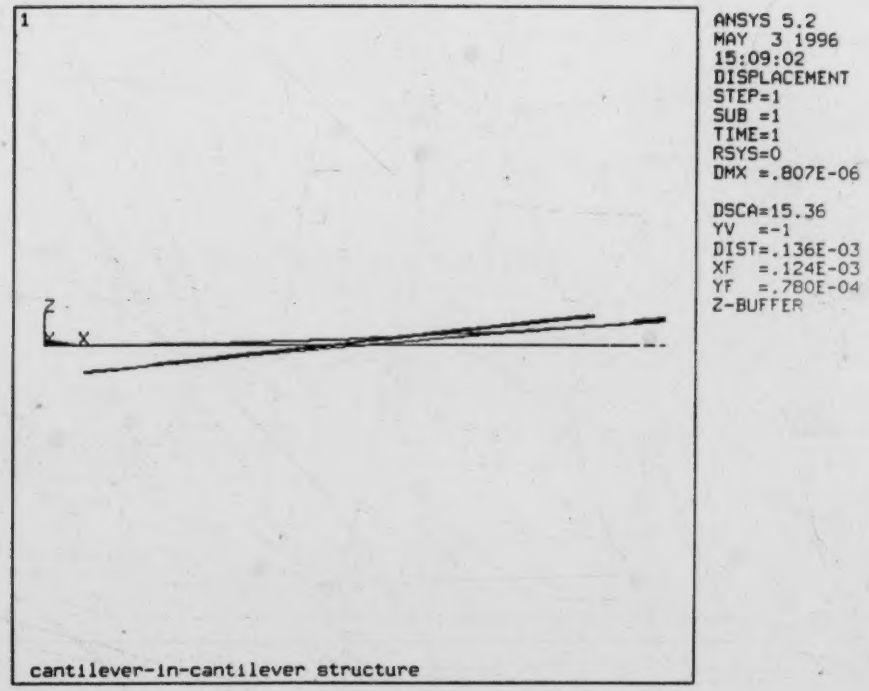


Figure 4.3 Deflection shape of a CIC structure

The deflection angle of the central mirror plate is about 0.51°. Displacements of every finite element node can be obtained after the simulation. The angle is calculated by:

$$\theta = \tan^{-1} \frac{d(z)}{d(x)}$$

in which *d(z)* is the maximum displacement obtained on the symmetric axis of the central plate which is parallel to the supporting arms, and *d(x)* is the difference between the x-

coordinates of the nodes with maximum z-displacement and with zero z-displacement on the symmetric axis. Comparing the simulation with experiment, the relative error is about 3%, which is quite acceptable. The error may be caused by regarding the aluminum and several silicon dioxide layers as a uniform layer composed of homogeneous material. Also, use of bulk values of parameters used in the simulation is another possible cause for error. Figure 4.4 is the comparison of ANSYS simulation with experiment. The experimental deflections are obtained using optical method and the maximum error bar is about 0.35° as discussed in Sec. 3.3.3.

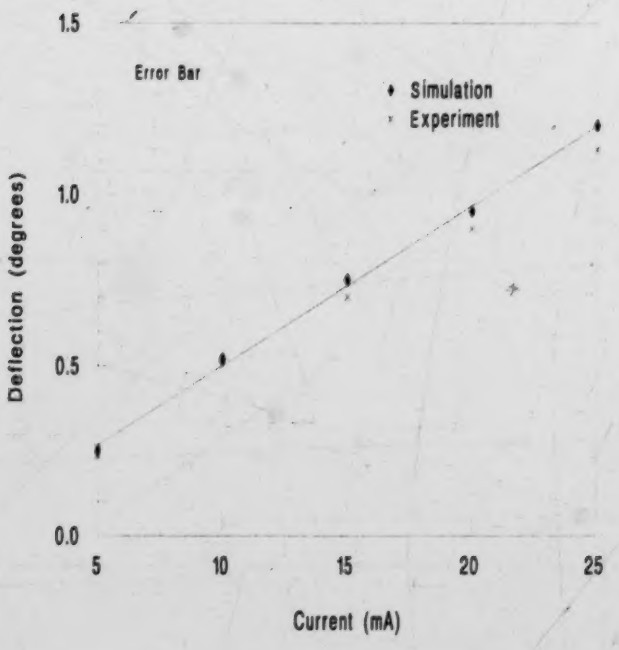


Figure 4.4 Comparison of ANSYS simulation with experiment

4.2 Resonant Vibration Analysis

ANSYS modal analysis is used to simulate the resonant vibration of the CIC devices. Modal analysis in the ANSYS program is a linear analysis. It can be used to determine the natural frequencies and mode shapes of a structure. The CIC device is built as a model composed of four layer shell elements (No. 91).

Table 4.1 compares the natural frequencies simulated by ANSYS and those obtained from experiment. The second column is the ANSYS results using bulk values of the material parameters and the third column is obtained using the adapted parameters. From the simulation results, we can see the bulk values of the material parameters can only be used with caution. The real values may be different.

Table 4.1 Natural frequencies of the triple CIC structures

	Experiment (kHz)	ANSYS Analysis (kHz)	
1	6.60	10.20	6.70
2	8.13	13.59	8.27
3	19.70	18.37	18.87
4	29.30	35.43	29.89
5			95.24

Comparing the first four resonant frequencies of the third column with the experimental results, the model built can be regarded as suitable. The maximum error is about 4%.

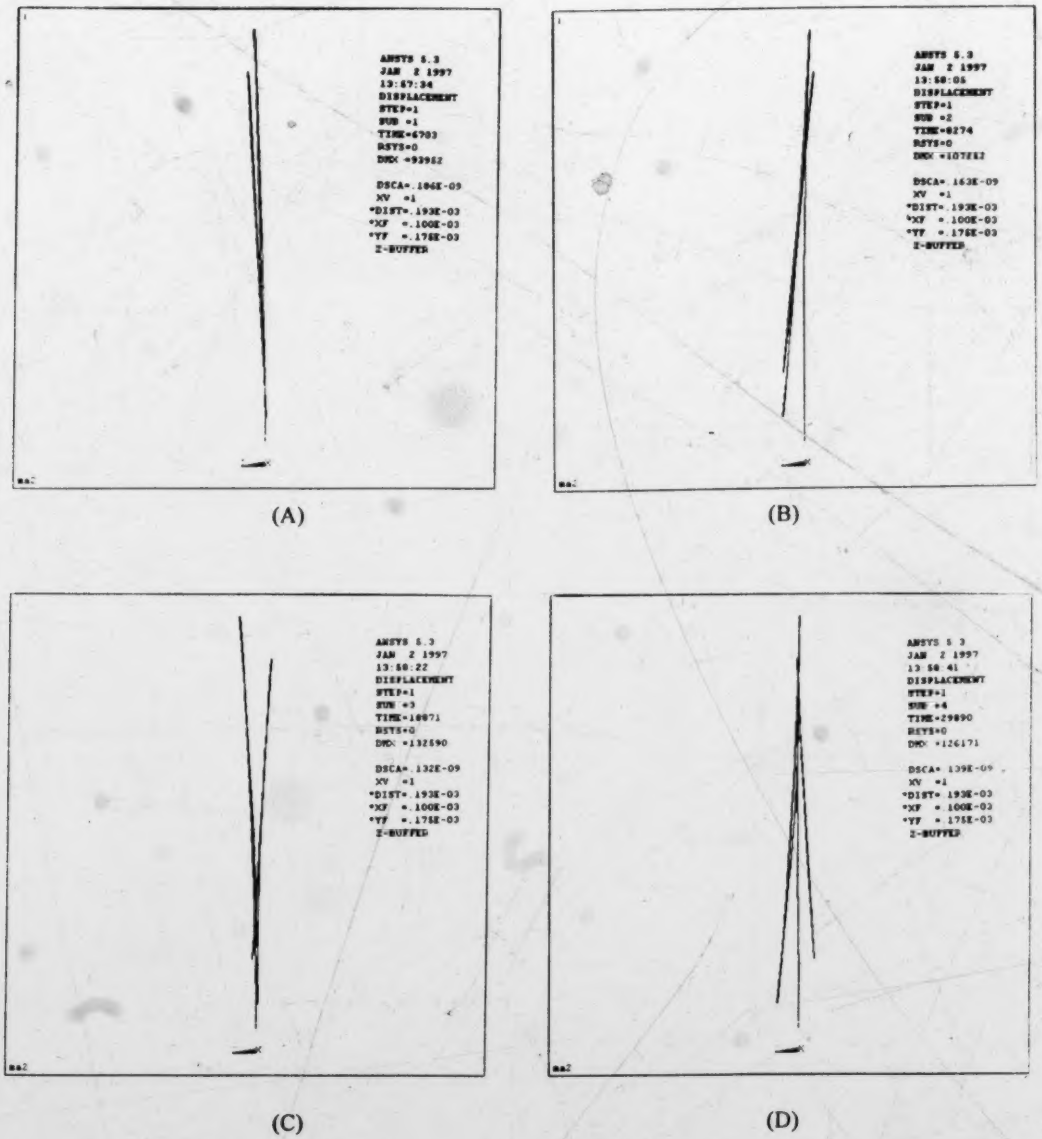


Figure 4.5 Vibration modes of triple CIC structure

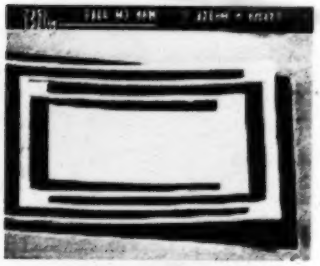
(A) f=6.70 kHz; (B) f=8.27 kHz; (C) f=18.87 kHz; (D) f=29.89 kHz

Four vibration modes are given in Figure 4.5. The vibration mode is different at different resonant frequency. Parts (a), (b), (c) and (d) of the figure correspond to the four vibration modes at the first four natural frequencies.

Through ANSYS modal analysis, a better understanding of the vibration characteristics of the CIC structures can be obtained. Relative positions of the three cantilevers of the CIC device are different in the different vibration modes. One can have more choice at which vibration mode is desirable, and which is not. For example, stresses of the structure under different modes may be studied to find a best vibration mode for piezoresistive detection method, which places a segment of piezoresistor at a certain position within the structure to detect the deflection. Details are given in the next chapter.

Moreover, the ANSYS modal analysis may be used as a starting point for further detailed transient dynamic analysis, which is, however, not within the scope of this thesis.

5



Piezoresistive Detection

The piezoresistance effect in silicon and germanium was discovered in 1954[39-40]. Piezoresistivity is a material property where the bulk resistivity is influenced by the mechanical stresses applied to the material. Because of the large piezoresistivity in monocrystalline silicon and polycrystalline silicon and their favorable mechanical behavior, piezoresistive silicon sensors have been widely used as pressure, acceleration and flow sensors etc.[41-45].

In our CMOS micromachining process, polysilicon, which is available through the standard CMOS IC fabrication, can be used as a piezoresistor. Placing a segment of polysilicon at a certain position within our CIC structure will permit the deflection of the device to be determined by measuring the resistance change of the polysilicon.

5.1 Piezoresistive Detection in CMOS Micromachining

In most applications of CMOS micromachining, we are interested in two cases of uniaxial stress applied to a detection resistor: the uniaxial stress applied (i) in the direction of the current through the resistors and (ii) perpendicular to the current. The two situations can be described using the longitudinal piezoresistive coefficient π_L and transversal piezoresistive coefficient π_T. The resistance change of the resistor due to small mechanical stresses is expressed as[46]:

$$\frac{\Delta R}{R} = \pi_L \Delta\sigma_L + \pi_T \Delta\sigma_T \qquad (5.1.1)$$

in which, σ_L and σ_T are stress components parallel and perpendicular to the current flow.

Figure 5.1 is the conceptual diagram of a CIC with a polysilicon piezoresistor embedded inside the supporting arms close to the clamped edges.

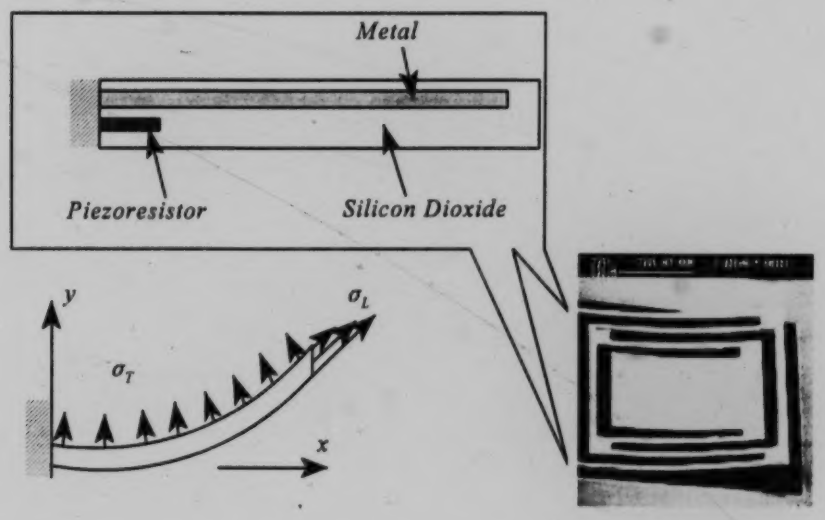


Figure 5.1 Conceptual diagram of a CIC structure with piezoresistor embedded inside the supporting arms

From the derivation of static deflection of a triple CIC structure in section 3.2.3, we can see the moment generated at the central cantilever is cascaded to the outer cantilever through the cantilevers in between, and the moments are enlarged at each stage. The maximum moment occurs at the clamped ends of the outer cantilever. That is also the position of the highest stresses and strains and represents the best location to place the piezoresistors. The polysilicon resistors are aligned parallel to the arms. In the case of the CIC vibrating at its resonant frequency, the stress component σ_L is modulated by the vibration and the change of stress component $\Delta\sigma_T$ is equal to zero. Assuming small deflections of the CIC structure and neglecting any 2ω contributions, the induced stress is proportional to the vibration amplitude $A \bullet \cos\omega t$:

$$\sigma_L = \sigma_{L,0} + \Delta\sigma_L \cdot \cos\omega t = \sigma_{L,0} + c \cdot A \cdot \cos\omega t \qquad (5.1.2)$$

The factor c between the oscillating stress component $\Delta\sigma_L$ and the vibration amplitude A depends on the actual structure and the exact location of the piezoresistors. Substituting $\Delta\sigma_L$ into equation (5.1.1), the resistance change is then:

$$\frac{\Delta R}{R} = \pi_L \cdot \Delta\sigma_L = \pi_L \cdot c \cdot A \qquad (5.1.3)$$

which means the changing of the vibration amplitude can be indicated by the changing of the piezoresistance. When the polysilicon piezoresistors are driven with a DC current I_0, the change in voltage across the piezoresistor is:

$$U = \Delta R \cdot I_0 = \frac{\Delta R}{R} \cdot R \cdot I_0 = c \cdot \pi_L \cdot A \cdot R \cdot I_0 \qquad (5.1.4)$$

With high sensitivity equipment, the vibration amplitude of the CIC structure can be obtained from the voltage change across the polysilicon piezoresistor.

5.2 Experimental Results

First the piezoresistor was measured under a static deflection. A DC current is supplied to the aluminum leads to actuate the device and another DC current from a constant current source (I_0=1.58 μA) is applied to the piezoresistor. An HP 34401A multi-meter is used to measure the voltage across the piezoresistance. The change in the resistance of the piezoresistor is then calculated by dividing the voltage across the piezoresistance by the constant current. An ohmmeter is not used here to prevent heating of the piezoresistor, since an ohmmeter can put out as much as 1 mA to measure resistance. Figure 5.2 shows the resistance change of the piezoresistor versus the input current of the aluminum.

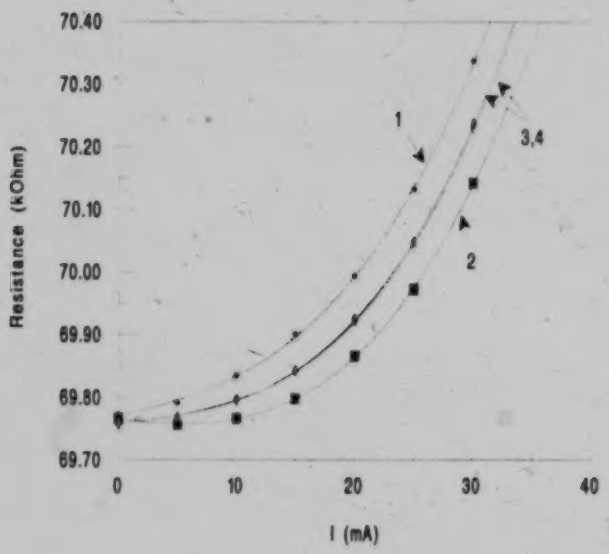


Figure 5.2 Piezoresistance versus current in aluminum lead

In Figure 5.2, curve 1 is for a current producing a deflection of the central cantilever out of the plane of substrate and 2 is corresponding to the current with opposite direction and produces a deflection down below the plane of the substrate. Curves 3 and 4 are obtained by measuring the deflection of the device without an external magnetic field and they reflect the thermal deflection and heating, since the polysilicon has a positive TCR. Figure 5.3 illustrates the resistance change of the piezoresistor getting rid of the thermal effects by subtracting the thermal values from the corresponding values of curves 1 and 2. The resulting data are least-squares fitted by straight lines.

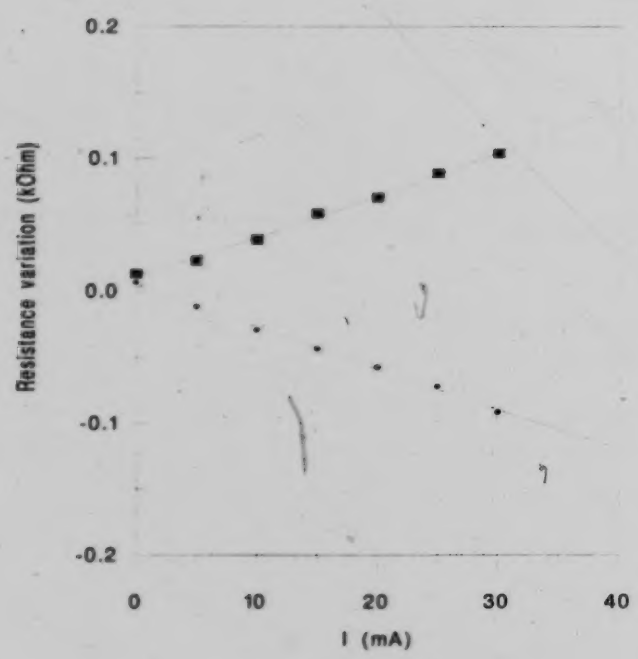


Figure 5.3 Resistance variation of piezoresistor without thermal effects

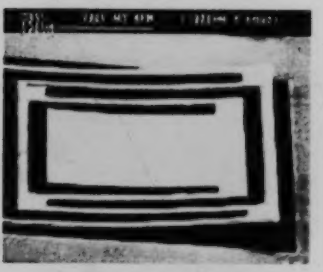
From Figure 5.3, we can see that the resistance change of the polysilicon within the current range from 0-40 mA is linear. But it is small, only about 0.06%, which makes it difficult to measure the resistance change of polysilicon during AC actuation. For AC actuation, no obvious resistance change can be observed using an oscilloscope. Failure may be due to the following two reasons:

(1) For polysilicon, the piezoresistive coefficients not only depend on the temperature and doping concentration, but also on the deposition conditions and annealing temperatures[47]. Therefore, the piezoresistive coefficients of different polysilicon layers have to be determined for each industrial IC technology used. Generally speaking, p-type polysilicon is preferred due to the properties of the anisotropic etching of silicon. P-type polysilicon has maximum piezoresistive coefficients in the <110> direction. But the chip discussed here is fabricated using the Mitel 1.5 micron regular process, which dopes poly1 and poly2 with phosphorus, which is n-type doping. This may be one reason for undetectable resistance change during AC actuation. The reason of choosing poly2 as piezoresistor is that poly2 has a smaller temperature coefficient of resistance, so that resistance change due to heating will be minimized.

(2) The neutral plane of a structure is the plane which has zero stress. The distance between poly2 and the neutral plane of the CIC device may not be large enough. The neutral plane of the CIC structure may be calculated using the method introduced in Sec. 3.3.2.2. The calculated neutral plane of a sandwich structure composed of one nitride layer, four oxide layers, one metal layer and one polysilicon layer is about 2.27 μm away from the substrate surface. The distance between the poly2 and substrate is about 1.0 μm. Thus, the distance from poly2 to the neutral plane of the structure is about 1.27 μm. Perhaps this distance is too short to produce sufficient stress on the poly2; further design and analysis needs to be done.

Also, some other methods may be used to enhance the piezoresistance change, like a Wheatstone bridge. Three piezoresistors can be carefully designed as comparison resistors in a Wheatstone bridge arrangement.

6



Conclusion and Outlook

A novel magnetically actuated CMOS micromachined Cantilever-In-Cantilever device has been introduced, characterized, and simulated in this thesis.

The work presented in this thesis contains four major parts: (1) Analytic estimation of the static deflection of the CIC structure; (2) Experimental characteristics; (3) ANSYS simulation of the static deflection and modal analysis; and (4) Piezoresistive detection discussion.

The static deflection of the CIC structure has been estimated. General equations for the displacement and deflection of n cascaded cantilevers have been given. The deflection of the CIC structure is linear with the actuating current, as predicted. Also, the CIC structure improves the deflection magnitude over the simple cantilever structure greatly under the same operating conditions.

A series of CIC structures has been tested and characterized. The analytic estimation gives good agreement with experimental results. Moreover, the resonant responses of the CIC structures have been measured and thermal effects on the CIC devices including a temperature phenomenon have been discussed.

Both static deflection and resonant response of the CIC devices have been simulated

using ANSYS. The simulation results also give good agreement with experiment.

Finally, a piezoresistive detection method has been considered and a 0.06% change of piezoresistance has been found under static deflection.

This is preliminary work. Further work may include:

- Optimize the structure. As mentioned in the thesis, some fabricated devices have a problem of incomplete etching. In micromachining, design rules of CMOS processes are violated intentionally to expose the silicon substrate. The drawback of the violation of design rules is that the yield after wet anisotropic etching is decreased seriously. The solution is to try to optimize the CIC devices according to some design rules which can satisfy both the designer and industrial foundries to increase the yield of etching.

- Reduce the size of the magnet. The magnetic field of the CIC actuation is provided by an external magnet, which is bulky compared to the actuator. Further development of the device may include the fabrication of a magnet on the silicon substrate by electroplating or other methods.

- Automate the experiment. Experimental work is still at its primary stage. Data acquisition and analysis need improvement. Computer aided data acquisition and analysis is also one of the future considerations.

- Improve the piezoresistive detection. The characteristics of polysilicon may be optimized through some custom processes. Special design may also improve the delectability of the polysilicon, e.g., Wheatstone bridge arrangement.

Some potential applications are given in Sec. 3.6. But it is by no means a complete list for the CIC devices. We hope some of them may come true in the near future.

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Appendix A: Splus program example for static deflection calculation (n=4)

** This Splus program is designed to calculate the static deflection of a quadruple CIC device according to equation (3.2.23). Deflections of other nCIC structures can be obtained by substituting n with the corresponding value.*

```
function (L, l, n)
{
################################
# L: the length of the supporting arms
# l: the length of the aluminum wire perpendicular to the external magnetic field
# m: The times of interpolations
# k: The initial sample size of given iid normal variables
#################################################################################
Theta<-rep(0,11)
f1<-rep(0,11)
f2<-rep(0,11)
FF<-rep(0,4)
M<-rep(0,4)
#L<-c(205, 240, 295, 370)
#l<-c(125, 285, 355, 425)
I<-seq(0, 50, 5)
B<-0.14
For (j in 1:11){
        Pi<-B * 0.001 * I[j] *l
        Icon<-10.9875 * 15
        E<-74 *0.001
        FF[1]<-Pi[1]
        for (i in 2:n){
                FF[i]<-Pi[i] - FF[(i-1)]
        }
        for (i in 1:n){
                M[i]<sum(FF[1:i] * L[1:i]
        }
        f1[j]<-sum(FF[1:n]*L[1:n]^2)/2
        f2[j]<-sum(M[1:(n-1)]*L[2:n])
        Theta[j]<- (f1[j] + f2[j]) / (E * Icon)
}
```

Appendix B: Input file for CIC ANSYS simulation

** This is the input file for ANSYS static simulation discussed in Chapter 4. A triple CIC device model has been built, element type, material properties and simulation conditions are all defined in this file. It may also be used for resonant response simulation by changing the analysis type to modal analysis.*

```
/title, cantilever-in-cantilever structure
/units, si
/prep7
! define half of the structure
rectng,0,236e-6,0,12e-6
rectng,28e-6,236e-6,28e-6,40e-6
rectng,28e-6,208e-6,56e-6,68e-6
rectng,44e-6,208e-6,84e-6,156e-6
rectng,16e-6,28e-6,28e-6,156e-6
rectng,208e-6,220e-6,56e-6,156e-6
rectng,236e-6,248e-6,0,156e-6
aglue,all
! define element type
et,1,91
! for shell91 keyopt(2)=1 is the only valid option for GUI
keyopt,1,2,1
! define real constant set 1
r,1
! define the layer number of element 91
rmodif,1,1,2,0
! define the thickness of two layers
rmodif,1,13,1,0,2.5e-6, 2.5e-6, 2.5e-6, 2.5e-6
rmodif,1,19,2,0,0.5e-6, 0.5e-6, 0.5e-6, 0.5e-6
! define material properties of silicon oxide
mp,ex,1,74e9
mp,dens,1,2.2e3
mp,nuxy,1,0.3
! define material properties of silicon nitride
mp,ex,2,320e9
mp,dens,2,2.8e3
mp,nuxy,2,0.25
! define element size
esize,8e-6,0
! mesh the area
asel,all
amesh,all
finish
! enter solver
/solu
! define analysis type
```

```
antype,0
! define the restraint
nsel,s,loc,x,0
d,all,all,0
! define the boundary condition
nsel,s,loc,y,156e-6
d,all,uy,0
! transfer solid model loads and boundary conditions to the finite element model
nsel,all
sbctran
eplot
/eof
```